(5) If the signal at the collector of Q7 is good, look at the collector of Q15 with the oscilloscope. You should see a 40 MHz signal at 2.3 V pk-pk (minimum). If the signal is bad, the problem must be Q15 and its associated components.

(6) If the signal at the collector of Q15 is good, check the TGC Attenuator as follows:

(a) CR29 should be forward biased by more than 0.5 V, and CR30 should not be forward biased by more than 0.4 V.

(b) If not, troubleshoot the CR29, CR30 circuitry.

(7) If the TGC Attenuator circuitry is good, the problem is in the IF Amplifier (Q17, Q18, and their associated components) or the Mixer circuitry (M1 etc.).

NOTE

To do signal tracing in this area, you need a high-impedance probe for your spectrum analyzer.

1A1A1-3

This fault code indicates that there is no 40 MHz IF output at J3 in the transmit AME mode.

Since the BIT test passed in USB mode, the problem has to be in that part of the circuitry that is unique to AME, which is Q8 and its associated components or CR19, CR20, and CR12. With AME selected, CR12 should be forward biased; CR19 and CR20 should be reverse biased.

1A1A1-4

This fault code indicates that there is no 40 MHz IF output at J3 in the transmit CW mode.

Since the BIT test passed in both USB and AME modes, the problem has to be in the circuitry that is unique to CW.

(1) Check the CW keyline circuitry as follows:

(a) Select CW mode on the transceiver.

(b) Check pin 10 of U2. When the transceiver is keyed with the CW key, this pin should go to +5 Vdc.

(c) If this is not the case, you have a keyline problem. The problem is most likely U1.

(2) Connect an oscilloscope to pin 15 of U3. Check for a 1 KHz signal at 50 mV pk-pk when the transceiver is keyed with the CW key.

(3) If the signal at pin 15 of U3 is bad, trace back through U3 and U2 to find the problem.

1A1A6-4

When you get this fault code, check the PPC light on the AGC/TGC Board. If the PPC light is on all the time when you key the transceiver in CW mode (with the CW key), then this fault code indicates that there is a problem in the 455 KHz Envelope Detector or in the TGC Attenuator.

Check the 455 KHz Envelope Detector as follows:

(1) Key the transceiver in CW mode with the CW key.

(2) Look at AR12 pin 1 with a DC voltmeter.

(3) If the voltage is +8 Vdc or less, the fault is probably in the 455 KHz Envelope Detector (CR17, AR12, and their associated components).

(4) If the voltage is greater than +8 Vdc, the problem is probably in the TGC Attenuator (CR28, CR29, CR30, and their associated components).

ADDITIONAL SYMPTOMS

The above fault codes cover the main signal path, but there are several other circuits on the Exciter PWB Assy that could cause problems. However, these circuits are readily identified by the following obvious symptoms:

LOW PWR Indicator Comes On When FWD Power Meter Indicates Full Output

The problem is probably in the LOW PWR Indicator circuitry: AR11A and its associated components. Also, check the adjustment of R254 (see the Alignments section).

Incorrect VOX, ANTIVOX Operation

Check AR4A, U6A, U6B, AR4B, and their associated components.

Incorrect CLIPPER Operation

Check AR8A, AR8B, U11A, and their associated components. The clipper level adjustment (R91) is preferential.

METER SELECT Inoperative

For the audio functions, check U18A, U18B, U18C, U17C, and their associated components. For power and VSWR functions, check U17A, U17B, and their associated components.

No PATCH Transmit Audio

Check U7A, U4C, and their associated components.

No PATCH Receive Audio

Check U7B, AR6A, and their associated components.

No NBSV Transmit Audio

Check T1, AR2B, U4B, and their associated components.

No LINE (REMOTE) Transmit Audio

Check AR2A, U4A, and their associated components.

No AFSK Transmit Audio

Check U3C and its associated components.

6-6. IF FILTER PWB ASSY, A1A2.

a. Preliminary Procedure.

(1) Remove the good IF Filter PWB Assy from the test-bed 100 Watt Transceiver, and replace it with the faulty IF Filter PWB Assy.

(2) Power up the transceiver.

(3) Check for the presence of the following power supply voltages on the board. Voltages should be within 0.5 V of the nominal value.

Voltage:	Measure at:
+15 Vdc	+ side of C38
-15 Vdc	- side of C40
+5 Vdc	+ side of C36

(4) If the voltages check good, run the receive-only BIT test.

b. Interpreting the BIT Codes. Use the fault codes listed below as a guide in troubleshooting the IF Filter PWB Assy. Refer to the section corresponding to the fault code you get. In the event that the test runs without generating a fault code, start at the beginning of the following procedures and work your way through to the end.

BIT Test Description for the IF Filter PWB Assy

(1) The BIT Oscillator on the Low Pass Filter Board is activated.

(2) Each filter is selected, and in each case the Synthesizer is used to center the BIT signal in each passband.

(3) The presence of the 455 KHz IF output is verified at J2 for each filter selected.

(4) If an AFSK Module is installed, the signal is sent to the AFSK filters via J5 and then returned at J6.

1A1A2-1

This fault code indicates that no IF signal (455 KHz) was detected at J5 on the IF Filter PWB Assy. The problem could be anywhere in the signal path (except for filters 2 and 3), the control circuitry, or the BIT Detector.

(1) Connect a signal generator to J1 on the IF Filter PWB Assy. Adjust it for a center frequency of 455 KHz at -20 dBm.

(2) Connect a spectrum analyzer to J2 on the IF Filter PWB Assy.

(3) Sweep the signal generator above and below the center frequency: 453 KHz to 457 KHz.

(4) Select USB on the transceiver, and check for a peak response on the analyzer at 454 KHz.

(5) Select LSB, and check for a peak response at 456 KHz.

(6) Select CW, and check for a peak response at 455 KHz.

(7) Check the gain of the board in USB mode, which should be about +17 dB at the peak filter response. The output signal at the analyzer should be about -13 dBm (this takes into account the 10 dB pad between the spectrum analyzer and the radio).

(8) If all three filters perform as expected (peak at the correct frequency and level), the BIT Detector circuit (Q6, Q7, Q8, and their associated components) is probably faulty.

(9) If two out of three filters perform as expected, then the remaining filter or its associated circuitry is at fault. In this case, check the output of the Filter Select Decoder, U1, and the outputs of the op amp. The following chart indicates which pin should be high for each filter selected:

	High	Low
FL1 (USB selected)	U1, pin 5	AR2, pin 1
FL2 (LSB selected)	U1, pin 6	AR1, pin 1
FL3 (CW selected)	U1, pin 7	AR1, pin 7

If the control voltages are good, then the filter is probably bad.

(10) If none of the filters performs as expected, check the outputs of U1 as indicated in step 9 above.

(11) Connect the spectrum analyzer to J5 on the IF Filter PWB Assy, and set the signal generator frequency to 455 KHz.

(12) Check for a gain of +23 dB, which corresponds to an output signal level of +13 dBm on the analyzer.

(13) If the signal is bad, the problem is in the Amplifier circuit (Q1, Q2, Q3, etc.). If the signal is good, troubleshoot the Impedance Matching circuit (Q4, Q5, and their associated components).

1A1A2-2, -3

These fault codes indicate a failure in a specific IF filter circuit (FL2 for 1A1A2-2 and FL3 for 1A1A2-3).

(1) Connect a signal generator to J1 on the IF Filter PWB Assy.

(2) Inject a -20 dBm test signal at 456 KHz (for fault code 1A1A2-2) or 455 KHz (for fault code 1A1A2-3).

(3) Select LSB (for fault code 1A1A2-2) or CW (for fault code 1A1A2-3), and check for the correct voltage levels at U1 and AR1. Refer to the chart below:

	High	Low
FL2 (LSB selected)	U1, pin 6	AR1, pin 1
FL3 (CW selected)	U1, pin 7	AR1, pin 7

(4) If the control voltages are good, check for the signal on both sides of the filter.

6-7. FIRST CONVERTER PWB ASSY, A1A3.

a. Preliminary Procedure.

(1) Remove the good First Converter PWB Assy from the test-bed 100 Watt Transceiver, and replace it with the faulty First Converter PWB Assy.

(2) Power up the transceiver.

(3) Connect a dummy load to the transceiver.

(4) Check for the presence of the following power supply voltages on the board. Voltages should be within 0.5 V of the nominal value.

Voltage:	Measure at:
+5 Vdc	L5
+15 Vdc	+ side of C87
-15 Vdc	- side of C85
+15 V-T (keyed)	L41
+15 V-R	L42

(5) If the voltages check good, run the receive-transmit BIT test.

b. Interpreting the BIT Fault Codes. Use the fault codes listed below as a guide in troubleshooting the First Converter PWB Assy. Refer to the section corresponding to the fault code you get. In the event that the BIT test runs without generating a fault code, start at the beginning of the following procedures and work your way through to the end.

BIT Test Description for the
First Converter PWB Assy

(1) Activates the BIT Oscillator signal and verifies the presence of receive IF output to the Receiver Board.

(2) In transmit, keys the transceiver in CW and verifies the presence of transmit RF output to the power amplifier.

1A1A3-1

This fault code indicates that the received signal level at the J2 output of the First onverter PWB Assy is incorrect or missing.

(1) Check the BIT Detector circuitry (Q7, AR1, Q8, and their associated components) as follows:

(a) Select USB mode, and set the operating frequency to 12.0000 MHz.

(b) Inject a -20 dBm RF signal into J1 at 12.001 MHz.

(c) Connect a spectrum analyzer to J2.

(d) Check for 40.454 MHz at -19 +/- 1 dBm on the analyzer (this value does not include the 10 dB attenuator pad).

(e) If the signal is good, check for a low (less than +0.5 Vdc) at the collector of Q8. If the collector of Q8 is not low, the problem is in the BIT Detector. If the collector of Q8 is low, the J6 connector is probably bad.

(2) If the signal at J2 is bad, then check TP1 with an oscilloscope. You should see the amplified First Local Oscillator signal (52.455 MHz) at 18 V pk-pk (minimum). If the signal at TP 1 is bad, the problem is in the Local Oscillator Amplifier (Q13-Q16 and their associated components.

NOTE

Check the DC levels of all the transistors before attempting to signal trace.

(3) If TP1 is good, check for the signal across R67 or R68. It should be 18 V pk-pk. If the signal is bad here, T4 is faulty or one of the Mixer transistors (Q17-Q20) is shorted. If the signal is good, proceed to step 4.

(4) Unsolder one end of JMP1. Connect the spectrum analyzer to pin 1 of J7. You should see the input signal (-20 dBm) with a slight loss (1 dB or so). If the signal is bad, signal trace between J1 and J7.

NOTES

Q1, Q3, and Q4 should be on during receive.

Q2 comes on during transmit and during receive when the signal coming in is too strong.

(5) If the signal is good at J7, do the following:

(a) Replace JMP1.

(b) Inject a 40.455 MHz signal into J3 at -40 dBm.

(c) Key the transceiver with the 2ND, TX KEY buttons on the front panel.

(d) Look at J4 on the spectrum analyzer. You should see the operating frequency at a level of -20 dBm or greater (not including any pad before the analyzer). If the signal is good, the IF Amplifier (Q6 and its associated components) must be bad. If the signal is bad, proceed to step 6.

(6) If the signal at J4 is bad, the problem is the Mixer or FL1. There are three possibilities:

Case 1: The signal is present but low (-20 to -40 dBm). The problem is more likely the Mixer. Change all four Mixer transistors.

Case 2: The signal is not present at all (less than -60 dBm). The problem is more likely the filter. Replace FL1.

Case 3: This is the gray area, where the signal is between -40 and -60 dBm. In this case, replace the Mixer transistors first. If the problem persists, replace the filter.

1A1A7-1

This fault code indicates that the output of the Second Receiver Mixer (on the Receiver Board) is bad. Normally, this means that the fault is on the Receiver Board. However, sometimes, if the signal out of the First Converter PWB Assy is weak, it will pass the BIT detector on that board but fail at the BIT detector on the Receiver Board.

Troubleshoot this fault code the same as fault code 1A1A3-1, except that you can skip step 1 (you can assume that the BIT detector is good and that the output from J2 is bad).

1A1A3-2

This fault code indicates that the RF transmit output from the First Converter PWB Assy to the Power Amplifier is bad.

(1) Check the transmit BIT Detector circuit as follows:

(a) Inject a 40.455 MHz signal into J3 at +4 dBm.

(b) Connect a spectrum analyzer to J4, with a 30 dB attenuator pad between the analyzer and J4.

(c) Key the transceiver with the 2ND, TX KEY buttons on the front panel.

(d) Check for a -12 dBm (this takes into account the 30 dB attenuator pad) signal (minimum) at the operating frequency on the spectrum analyzer.

(e) If the signal is good, check for a low (less than +0.5 Vdc) at the collector of Q12. If Q12's collector is low, then the J4 connector is probably bad. If Q12's collector is high, then the BIT Detector circuit (Q11, Q12, and their associated components) is bad.

(2) If the signal at J4 is bad, then the problem has to be one of the following:

pin diode switch CR10, CR11

pin diode switch CR7, CR8

amplifiers Q9, Q10, or their associated components

(a) Check the diodes first. In transmit, CR10 should be forward biased and

CR11 should be reverse biased. CR8 should be forward biased, and CR7 should be reverse biased.

(b) If the diodes check good, then the problem is in the Amplifier circuit: Q9, Q10, and their associated components.

1A1A4-1

This fault code indicates that the output from the Power Amplifier is bad. However, if the output from the First Converter PWB Assy is weak, it may pass the BIT detector on this board but may be insufficient to drive the Power Amplifier to its rated output.

Troubleshoot this fault code as follows:

(1) Set up a test signal as in step 1 of the 1A1A3-2 fault code procedure.

(2) Verify that the output of J4 is bad.

(3) Proceed as in step 2 of the 1A1A3-2 fault code procedure.

6-8. POWER AMPLIFIER ASSY, A1A4.

a. Preliminary Procedures.

(1) Visual inspection

(a) Check the Power Amplifier PWB Assy for damaged components.

(b) Check for pieces of metal lodged between the board and the heat sink.

(2) Resistance measurements

(a) Using the R x 1 scale on a Simpson 260 Multimeter, check for a resistance of more than 100 ohms between E13 (+13.2 Vdc supply line) and ground. If the measurement indicates a short circuit, check to see whether Q8 and Q10 are insulated from the heat sink.

(b) Check for a resistance of more than 20 ohms between TP2 (+5.5 Vdc line) and ground.

If this measurement indicates a short circuit, check for a possible solder short along the +5.5 Vdc line.

(c) Check for a short circuit between E13 and the collectors of Q1 through Q5.

If there is no continuity between E13 and the collector of Q1, check R65 and T2 to see if they are open.

If there is no continuity between E13 and the collector of Q2 or Q3, check R66, T4, and the 18 AWG jumper wire between E18 and E19.

If there is no continuity between E13 and the collector of Q4 or Q5, check R67, T6, and the 14 AWG jumper wires between E20 and E21 and between E1 and E22&

b. Alignment Procedures.

Do the alignment procedures for the Power Amplifier in Section II of this chapter. These may help to isolate or correct a fault.

c. Troubleshooting the Power Amplifier.

If the above procedures do not isolate problems in the Power Amplifier, here are a few other things you can do:

(1) If you cannot drive the Power Amplifier to full output power at 30 MHz, check the RF Detector/VSWR Protection circuit.

(a) Measure the voltage at TP4. At full output power, this voltage should be approximately +4 Vdc.

(b) If the TP4 voltage is bad, then the problem is most likely in the RF Detector circuit.

(c) If the TP4 voltage checks okay, the RF Detector should be all right. Check the VSWR Protection circuit. The output of U1A, pin 1, should not be +4 Vdc unless J7 is not terminated in a 50-ohm load.

(2) You can use an oscilloscope to check the base-to-collector signal gain for the pre-driver (Q1), drivers (Q2 and Q3), and final amplifiers (Q4 and Q5). Even though the signals are not pure sinewaves, there should be at least a 2:1 signal gain at each of these stages.

(3) To check any of the above transistors, unsolder the base lead(s) and check the transistor with an ohmmeter.

(4) If the Power Amplifier's performance varies significantly with temperature, check the bias control circuits for the drivers (Q2 and Q3) and final amplifiers (Q4 and Q5).

6-9. LOW PASS FILTER PWB ASSY, A1A5.

a. Preliminary Procedure.

(1) Remove the good Low Pass Filter PWB Assy from the test-bed 100 Watt Transceiver, and replace it with the faulty Low Pass Filter PWB Assy.

(2) Connect a dummy load to the output (J1) of the 100 Watt Transceiver.

(3) Power up the transceiver.

(4) Check for the presence of the following power supply voltages on the board. Voltages should be within 0.5 V of the nominal value.

Voltage:	Measure at:
+13.6 Vdc	L24
+15 Vdc	L25
-15 Vdc	L27
+13.6 V-A	L43
+13.6 V-B	L44

(5) If the voltages check good, run the receive-transmit BIT test.

b. Interpreting the BIT Fault Codes. Use the fault codes listed below as a guide in troubleshooting the Low Pass Filter PWB Assy. Refer to the section corresponding to the fault code you get. In the event that the test runs without generating a fault code, start at the beginning of the following procedures and work your way through to the end.

BIT Test Description for the Low Pass Filter PWB Assy

(1) The BIT Oscillator on the Low Pass Filter PWB Assy is activated.

(2) With all filters deselected, RF output is checked at J3. There should be no RF output.

(3) RF output is checked again with each filter selected in turn.

(4) If all filters pass this portion of the test, RF output is checked with all filters deselected again. This ensures that none of the relays is sticking.

(5) Band 6 is then selected, and the Synthesizer is set to receive the BIT Oscillator signal.

(6) In transmit, the transceiver is keyed in CW mode; and the RF output is checked by sampling it at J6.

1A1A5-1

This fault code indicates that the BIT Oscillator signal was not detected by the Receive BIT Detector at the J3 output. In the following steps, we will manually activate the BIT Oscillator signal and trace it through the board.

(1) On J7, remove the jumper from pins 1 and 2 and insert it on pins 2 and 3.

(2) Set the transceiver for a frequency of 2.456 MHz USB.

(3) Listen for a tone with a signal strength of 16-19 segments on the front panel FWD meter.

(4) If the tone is audible and of the correct strength, the problem has to be in the BIT ENABLE line (J5, pin 13; R40; C186) or in the Receive BIT Detector.

(5) If the tone is not audible, do the following:

(a) Visually check relays K1 and K7. They should be closed.

(b) Check for +13.6 Vdc on both sides of L43 and L44.

(c) Check the BIT ENABLE line. There should be a logic HI on pin 7 of J5 and pin 3 of U1; there should be a logic LO on pin 14 of U1.

(d) Check to see whether K14 is closed--it should be.

(e) Check for the presence of the BIT signal (~60 mV pk-pk) at the + side of C207. If the signal is not present, either the BIT Oscillator is not working or there is a short on the signal line--trace all the way back to J3 for shorts.

(f) Check for the presence of the BIT signal (~60 mV pk-pk) at J8, pin 3.

(g) Check for the presence of the BIT signal (~50-60 mV pk-pk) at K1, pin 5.

(h) Check for the presence of the BIT signal (approximately 50-60 mV pk-pk at J3. If the signal is not present here, but present everywhere else, K13 is probably open.

1A1A5-2 through 1A1A5-6

One of these fault codes indicates that the BIT Oscillator signal failed to pass through a specific filter (the fault code corresponds to the number of the filter; for example, 1A1A5-4 corresponds to filter 4). The fact that 1A1A5-1 was not declared indicates that all the common circuitry is good. Therefore, the problem must be in the specific filter or the relays controlling it.

(1) Manually activate the BIT Oscillator by moving the jumper on J7 from pins 1 and 2 to pins 2 and 3.

(2) Set the transceiver to a frequency in the faulty band. Refer to the following chart:

Band	Frequency range
2	2.6 - 4.19999 Mhz
3	4.2 - 6.79999 MHz
4	6.8 - 10.99999 MHz
5	11.0 - 17.99999 MHz
6	18.0 - 29.99999 MHz

(3) Visually check to see whether the associated relays at either end of the suspected filter are energized. Use the following chart:

Filter	Input relay	Output relay
2	K8	K2
3	K9	K3
4	K10	K4
5	K11	K5
6	K12	K6

(4) If both relays do not energize, check the control line for the suspected filter and the associated relay driver (U1).

(5) If the relays energize, signal trace the suspected filter. Signal strength should be approximately 50-60 mV pk-pk.

1A1A5-7

This fault code indicates that one set of filter relays remained stuck in the energized position after being commanded off. (The BIT circuitry checked for the presence of the test signal at the Receive BIT Detector after all the filters were deselected.) The following procedure manually checks the operation of each set of relays.

(1) On the front panel of the transceiver, step through all six frequency bands. As you change from one band to the next, visually check to see that the proper set of relays deenergizes and the proper set of relays energizes. Use the following chart and the component location drawing (figure 6-6) for the Low Pass Filter PWB Assy.

Filter Band	Frequency Range	Relays Energized
1	1.6 - 2.59999 MHz	K1, K7
2	2.6 - 4.19999 MHz	K2, K8
3	4.2 - 6.79999 MHz	K3, K9
4	6.8 - 10.99999 MHz	K4, K10
5	11.0 - 17.99999 MHz	K5, K11
6	18.0 - 29.99999 MHz	K6, K12

(2) For example, when switching from a frequency in Band 2 to one in Band 3, relays K2 and K8 should deenergize (contacts open), and relays K3 and K9 should energize (contacts close).

(3) When you find the set of relays that does not open when it is supposed to, check the control line and driver circuitry for that set.

1A1A5-8

This fault code occurs during the transmit phase of the BIT test. From a comparison of the voltages at J6 (V REFL, V FWD), the test determines whether the VSWR is abnormally high.

(1) Check that K13 (the transmit/receive relay) energizes when you key the transceiver.

(2) If K13 does not function properly, check the T/R Relay Control circuit.

(3) Disconnect the cable at J2 on the Low Pass Filter PWB Assy. Insert a T-connector between J2 and a dummy load. Connect the other end of the T-connector to an RF voltmeter.

(4) Set the transceiver for AME mode.

(5) Key the transceiver with no modulation.

(6) Check for ~35 Vac on the RF voltmeter.

(7) If there is no power output, check for a short between J1 and K13 or between J2 and K14.

(8) If you do get the required amount of power out, check the Directional Coupler circuit (secondary side of T1). This circuit is evidently sending out erroneous information to the BIT circuitry via J6.

1A1A5-9

This fault code indicates that there is no power out of the Low Pass Filter PWB Assy in transmit.

Troubleshoot this fault code the same way as fault code 1A1A5-8.

6-10. AGC/TGC PWB ASSY, A1A6.

a. Preliminary Procedure.

(1) Remove the good AGC/TGC PWB Assy from the test-bed 100 Watt Transceiver, and replace it with the faulty AGC/TGC PWB Assy.

(2) Connect a dummy load to the output (J1) of the transceiver.

(3) Power up the transceiver.

(4) Check for the presence of the following power supply voltages on the board. Voltages should be within 0.5 V of the nominal value, except for the +10 Vdc, which should be within 0.25 V of the nominal value.

Voltage:	Measure at:
+5 Vdc	+ side of C6
+15 Vdc	+ side of C7
+15A	+ side of C62
-15 Vdc	- side of C8
-15A	- side of C64
+10 Vdc	AR3 pin 1

(5) If the voltages check good, run the receive-transmit BIT test.

b. Interpreting the BIT Codes. Use the fault codes listed below as a guide in troubleshooting the AGC/TGC PWB Assy. Refer to the section corresponding to the fault code you get. Note that the fault codes are divided into two groups: AGC fault codes and TGC fault codes. This is because the AGC and TGC are completely different and separate functions. They have nothing to do with each other except for their use of the same power supply voltages. In the event that the test runs without generating a fault code, start at the beginning of the following procedures and work your way through to the end.

BIT Test Description for the AGC/TGC PWB Assy

AGC Section (Receive Portion of the BIT Test)

(1) Checks signal strength (looks for 16-19 segments on the "S" meter) in USB at maximum RF gain with the BIT Oscillator (on the Low Pass Filter PWB Assy) activated.

(2) Checks signal strength in USB at maximum RF gain with the BIT Oscillator not activated.

(3) Checks signal strength in USB at minimum RF gain with the BIT Oscillator activated.

TGC Section (Transmit Portion of the BIT Test)

(4) Keys the transceiver in CW mode.

(5) Verifies the correct transceiver output power level.

(6) Verifies that the TGC system has stabilized at a normal control level.

AGC Fault Codes

1A1A6-1

This fault code indicates that the AGC voltage is too high.

(1) Rotate the RF gain control on the front panel of the transceiver fully clockwise.

(2) Disconnect the antenna from the transceiver so that no signal is coming in.

(3) Check the following test points for the indicated voltages. (Measurements should be taken with the medium AGC speed selected.)

Test Point	Voltage (+/- 0.5 Vdc)
TP11 (AGC threshold)	-7 Vdc
TP12 (AGC delay)	0 Vdc
TP13 (combined AGC)	0 Vdc
TP15 (2nd IF AGC)	0 Vdc
TP16 (1st IF AGC)	-6 Vdc
TP17 (RF AGC)	0 Vdc

Record your readings.

(4) On the Low Pass Filter PWB Assy, manually activate the BIT Oscillator by placing the jumper on J7 into the test position (pin 2 to pin 3).

(5) Select 2.456 MHz USB on the transceiver.

(6) Check the test points again, and compare the results with the values listed below:

Test Point	Voltage (+/- 0.5 Vdc)
TP11 (AGC threshold)	+6.6 Vdc
TP12 (AGC delay)	+6.6 Vdc
TP13 (combined AGC)	+6.6 Vdc
TP15 (2nd IF AGC)	-3.8 Vdc
P16 (1st IF AGC)	+5.3 Vdc
TP17 (RF AGC)	0 Vdc

Record your readings.

(7) Use the test point readings to isolate the problem.

A1A1A6-2

This fault code indicates that there is no manual RF gain control; that is, the AGC voltages do not vary correctly as the sensitivity of the transceiver goes from maximum to minimum.

(1) Rotate the RF GAIN control on the front panel of the transceiver fully clockwise.

(2) Disconnect the antenna from the transceiver so that no signal is coming in.

(3) Measure the voltage at TP13. It should be 0 Vdc.

(4) Rotate the RF GAIN control fully counterclockwise. The voltage at TP13 should now be approximately +9.6 Vdc or more.

(5) If this is not the case, check AR22A and its associated circuitry.

1A1A7-4

This fault code indicates that the AGC set point is bad.

Perform the AGC Threshold Adjustment (R167). If the fault persists, troubleshoot this fault code the same way as fault code 1A1A6-1.

TGC Fault Codes

1A1A6-3

This fault code indicates that the TGC set point is incorrect, as indicated by an out-of-tolerance reading on the forward power meter. In other words, the microprocessor reads the voltage on pin 16 of J1, which is a buffered sample from the VSWR bridge on the Low Pass Filter PWB Assy, to determine whether the output power (and therefore the TGC set point) is correct.

The problem could be anywhere in the TGC circuitry. Refer to the flowchart (figure 6-18).

1A1A6-4

This fault code indicates that the TGC output voltage has not stabilized at a normal control level.

The problem could be anywhere in the TGC circuitry. Refer to the flowchart (figure 6-18).

All Other Fault Codes

Normally, no fault codes other than the above should be declared during the TGC (transmit) portion of the BIT test. Therefore, when a fault code other than 1A1A6-3 or 1A1A6-4 is declared (when the AGC/TGC PWB Assy is known to be bad), the most likely suspects are the PPC circuitry and the output comparator (AR13B, Q10, and Q11).

Check the emitter of Q9 to ensure that it is at +2.7 Vdc +/- 200 mV. If the voltage is higher than that and the PPC LED is not lit, suspect a problem with Q9. If the PPC LED is lit, check out the PPC circuitry (see pages 1 and 2 of the flowchart).

6-11. RECEIVER PWB ASSY, A1A7.

a. Preliminary Procedure.

(1 Remove the good Receiver PWB Assy from the test-bed 100 Watt Transceiver, and replace it with the faulty Receiver PWB Assy.

(2) Power up the transceiver.

(3) Connect a dummy load to the transceiver.

(4) Check for the presence of the following power supply voltages on the board. The voltages should be within 0.5 V of the nominal value.

Voltage:	Measure at:
+5 Vdc	+ side of C141
+15 Vdc	+ side of C4
-15 Vdc	- side of C142
+13.6 Vdc	+ side of C140
+15 V-R	+ side of C12 (in receive)
+15 V-T	+ side of C14 (in transmit)

(5) If the voltages check good, run the receive-transmit BIT test.

b. Interpreting the BIT Fault Codes. Use the fault codes listed below as a guide in troubleshooting the Receiver PWB Assy. Refer to the section corresponding to the fault code you get. In the event that the BIT test runs without generating a fault code, look for other obvious symptoms, such as no speaker audio or no sidetone. Then refer to the "ADDITIONAL SYMPTOMS" section following the BIT code sections.

BIT Test Description for the Receiver PWB Assy

1. Checks for the presence of the board by sending data to the board and receiving the MCB loop back bit in return.

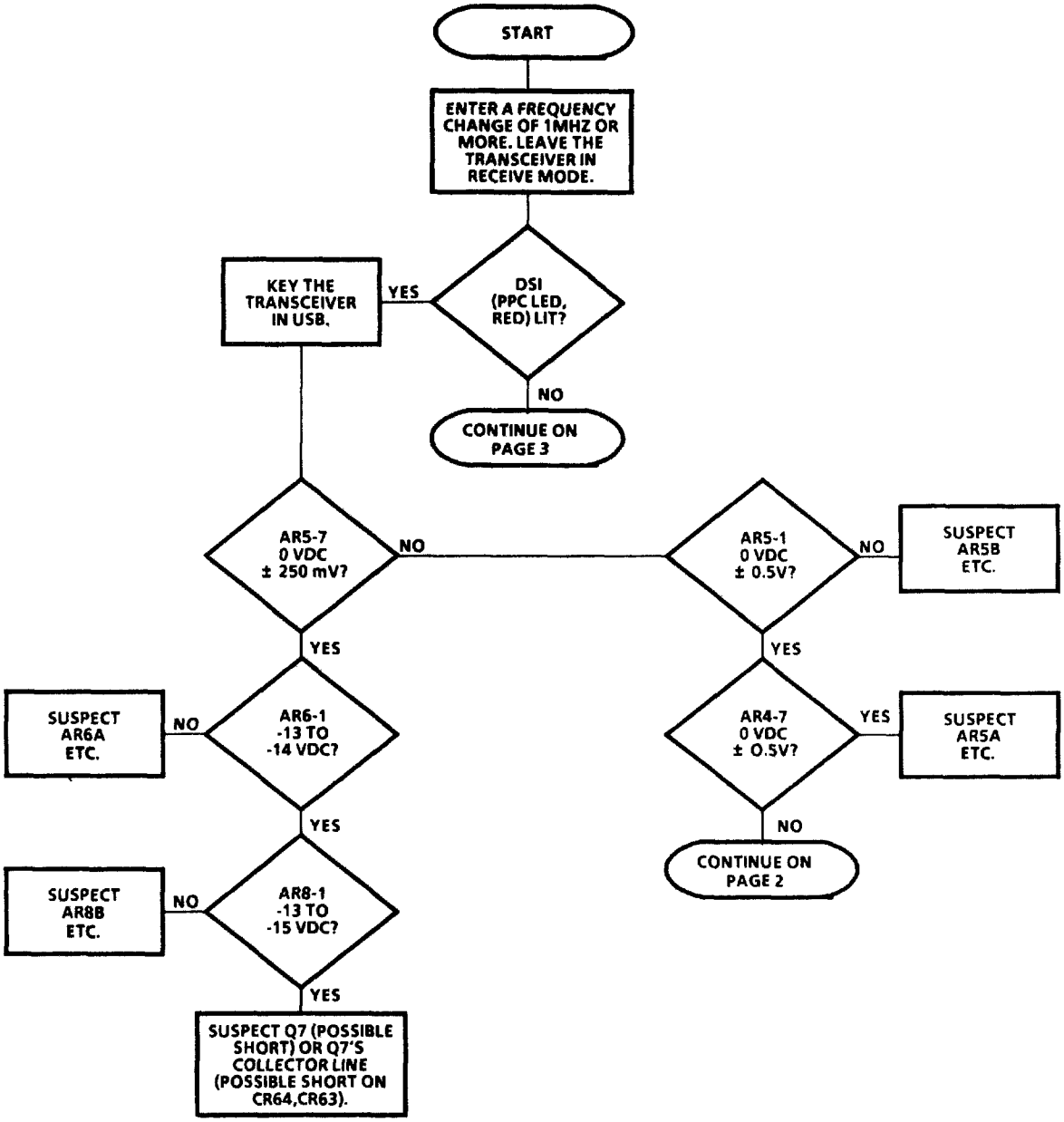
2. Disables the speaker by turning on Q27 and disables the LINE output by turning off CR38.

3. Activates the BIT Oscillator and verifies the presence of 455 KHz IF at J2 (output to IF Filter PWB Assy).

4. Bypasses the volume and squelch controls, sets the RF gain to maximum, and verifies that no LINE audio is present in USB.

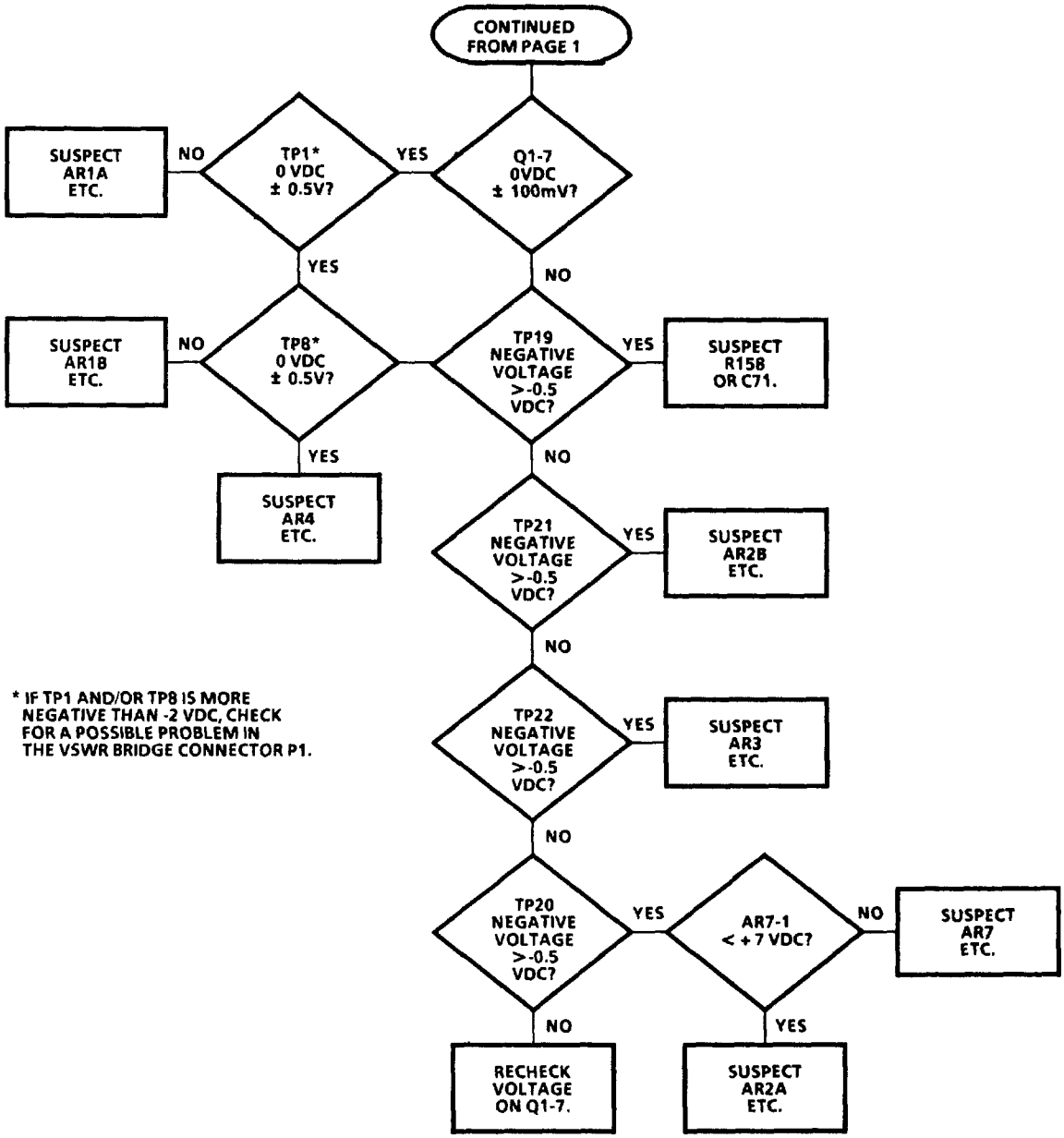
5. Activates the BIT Oscillator and verifies the presence of LINE audio.

6. In transmit, verifies the presence of 455 KHz IF at J2 (output to IF Filter PWB Assy).



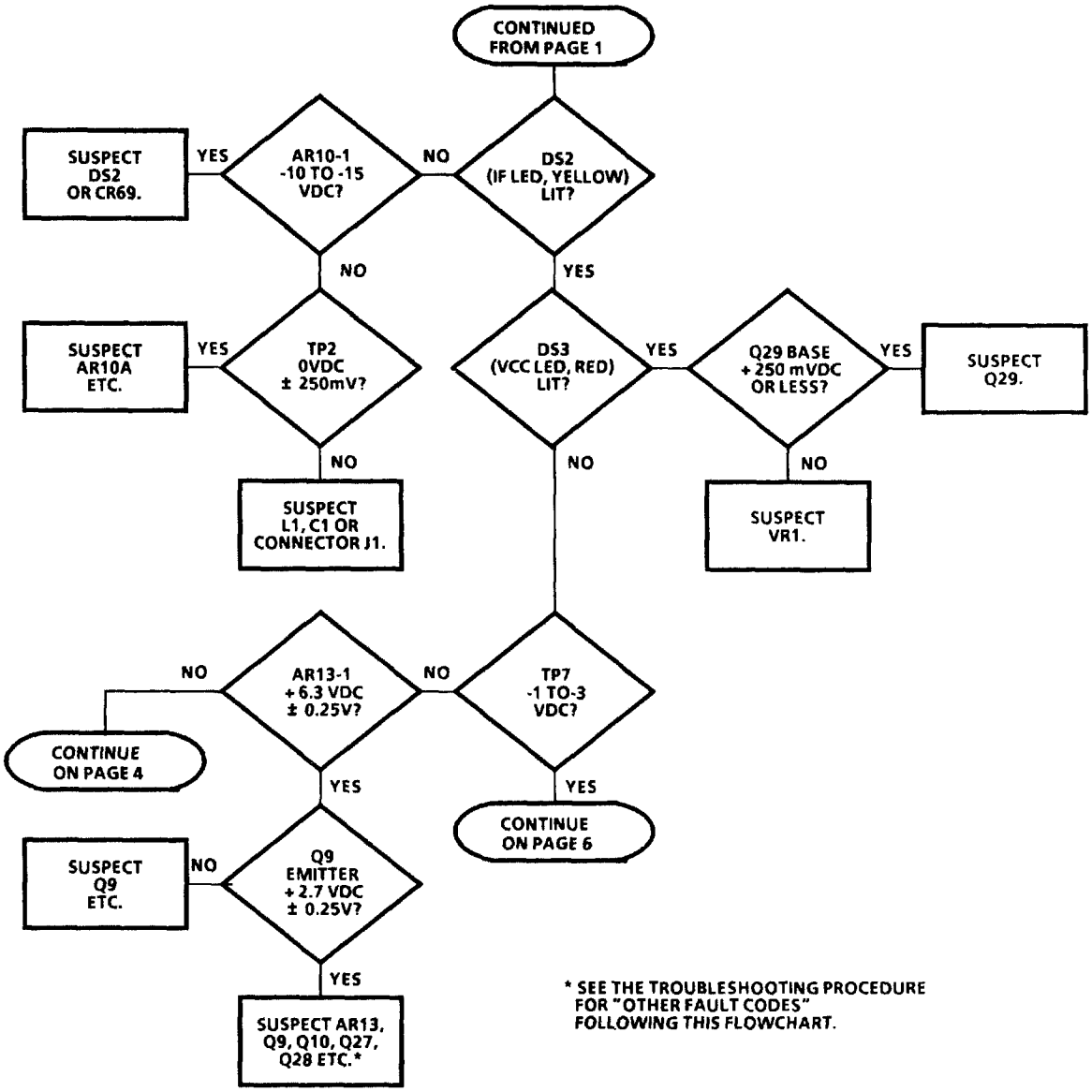
*350-135-1

Figure 6-18. TGC Fault Isolation Chart (Page 1 of 15)



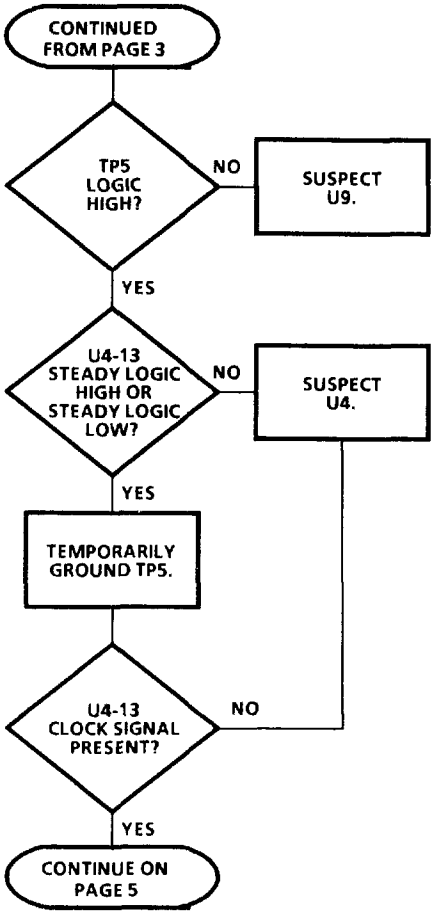
*350-135-2

Figure 6-18. TGC Fault Isolation Chart (Page 2 of 15)



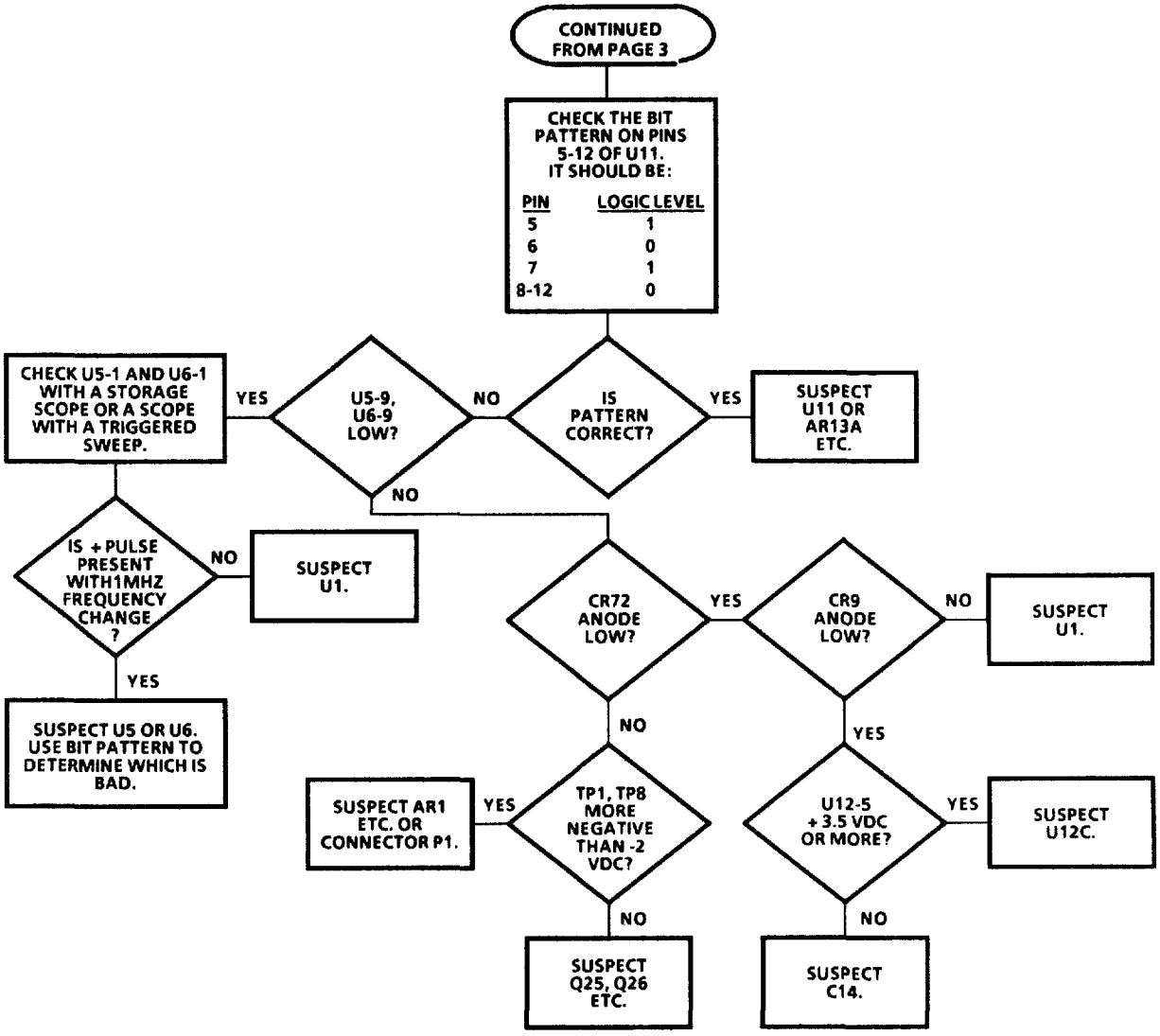
*350-135-3

Figure 6-18. TGC Fault Isolation Chart (Page 3 of 15)



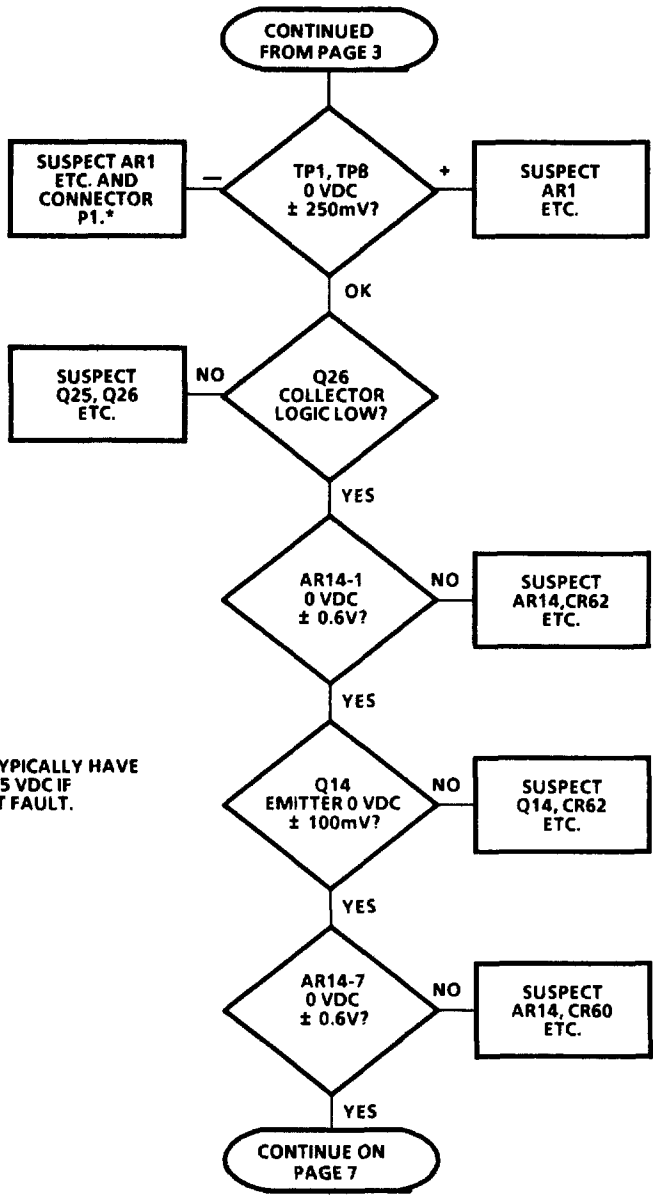
*350-135-4

Figure 6-18. TGC Fault Isolation Chart (Page 4 of 15)



*350-135-5

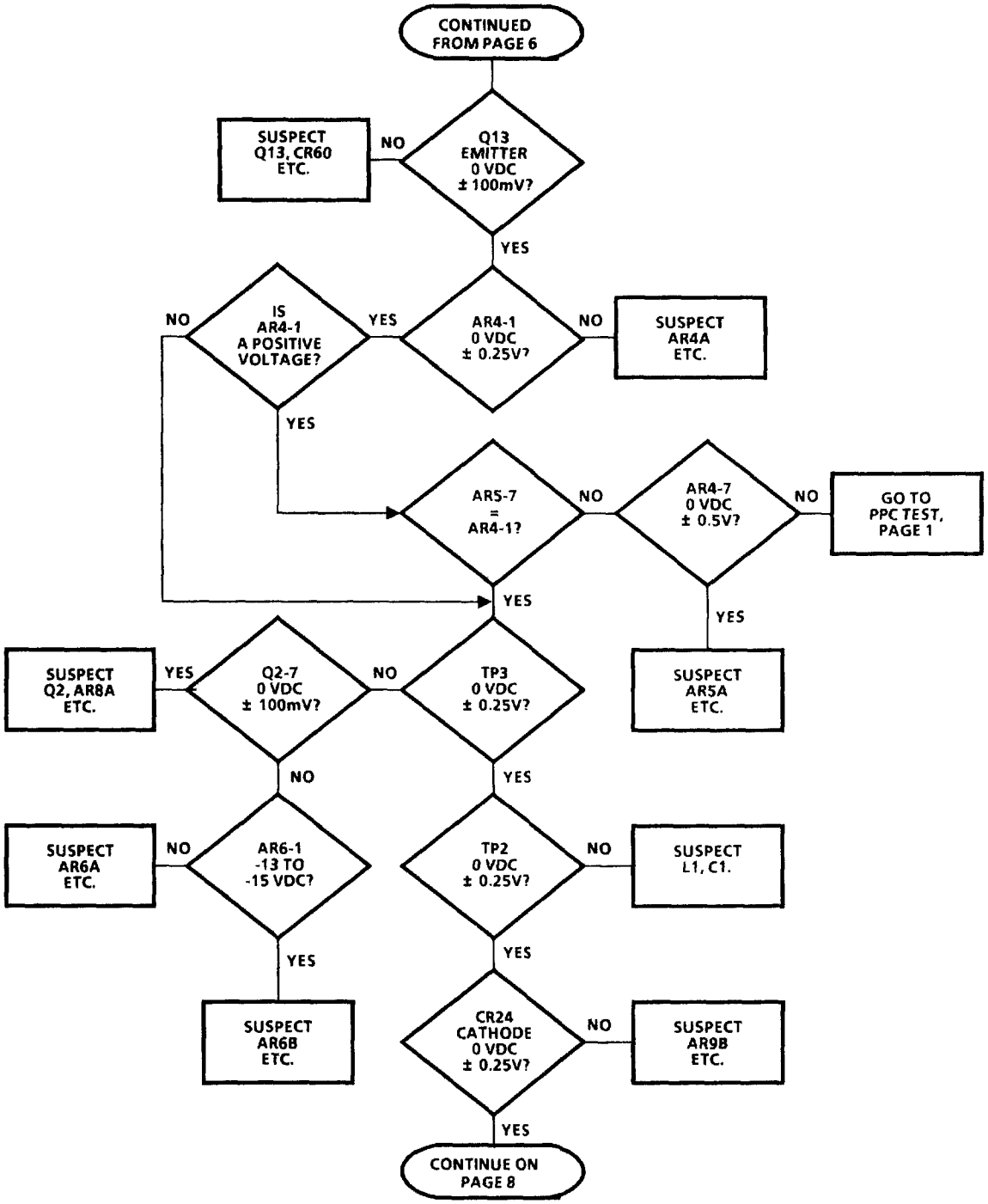
Figure 6-18. TGC Fault Isolation Chart (Page 5 of 15)



* TP1 AND TP8 WILL TYPICALLY HAVE APPROXIMATELY-2.5 VDC IF CONNECTOR P1 IS AT FAULT.

*350-135-6

Figure 6-18. TGC Fault Isolation Chart (Page 6 of 15)



*350-135-7

Figure 6-18. TGC Fault Isolation Chart (Page 7 of 15)

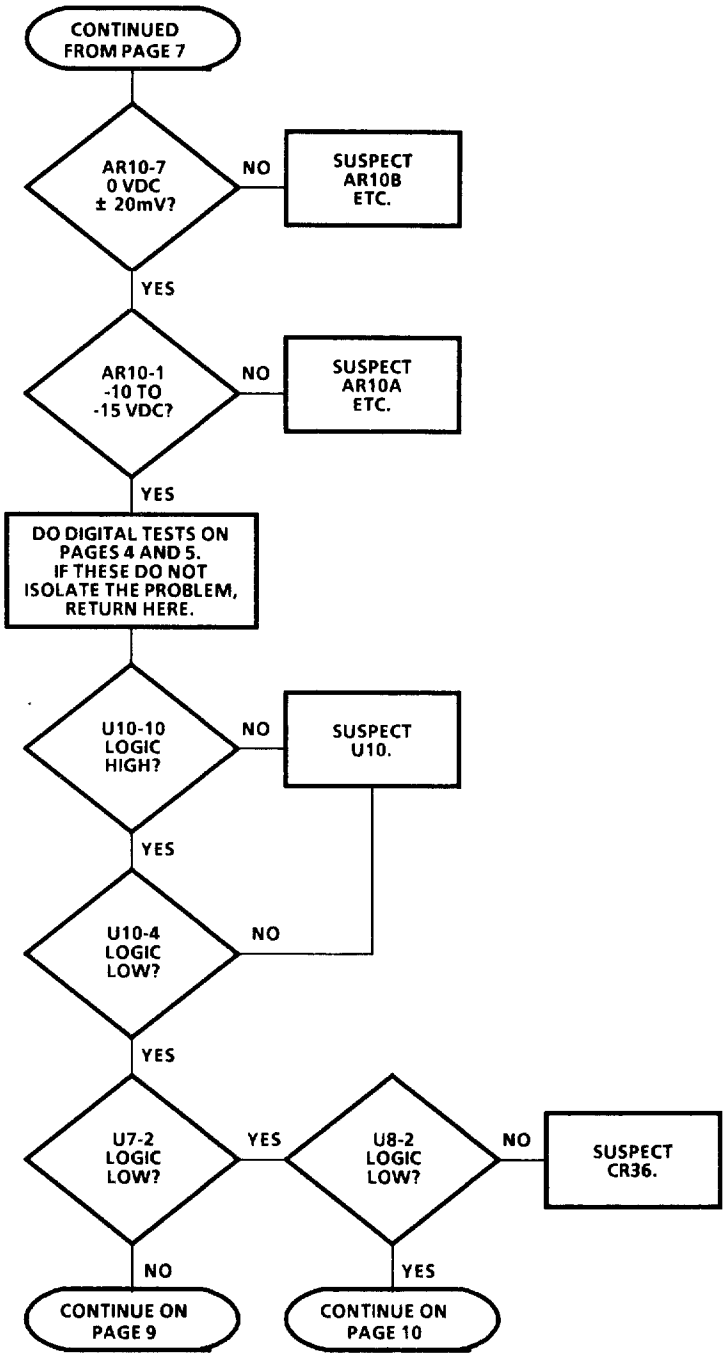
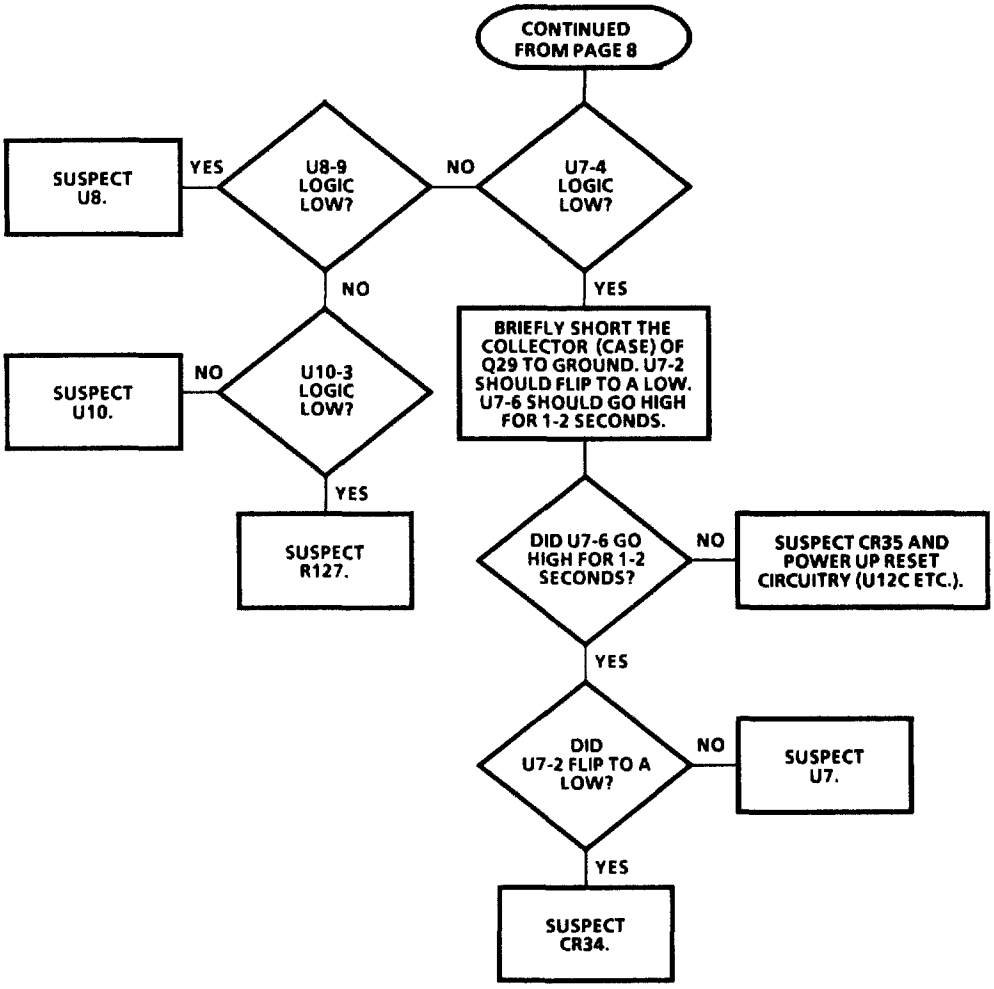
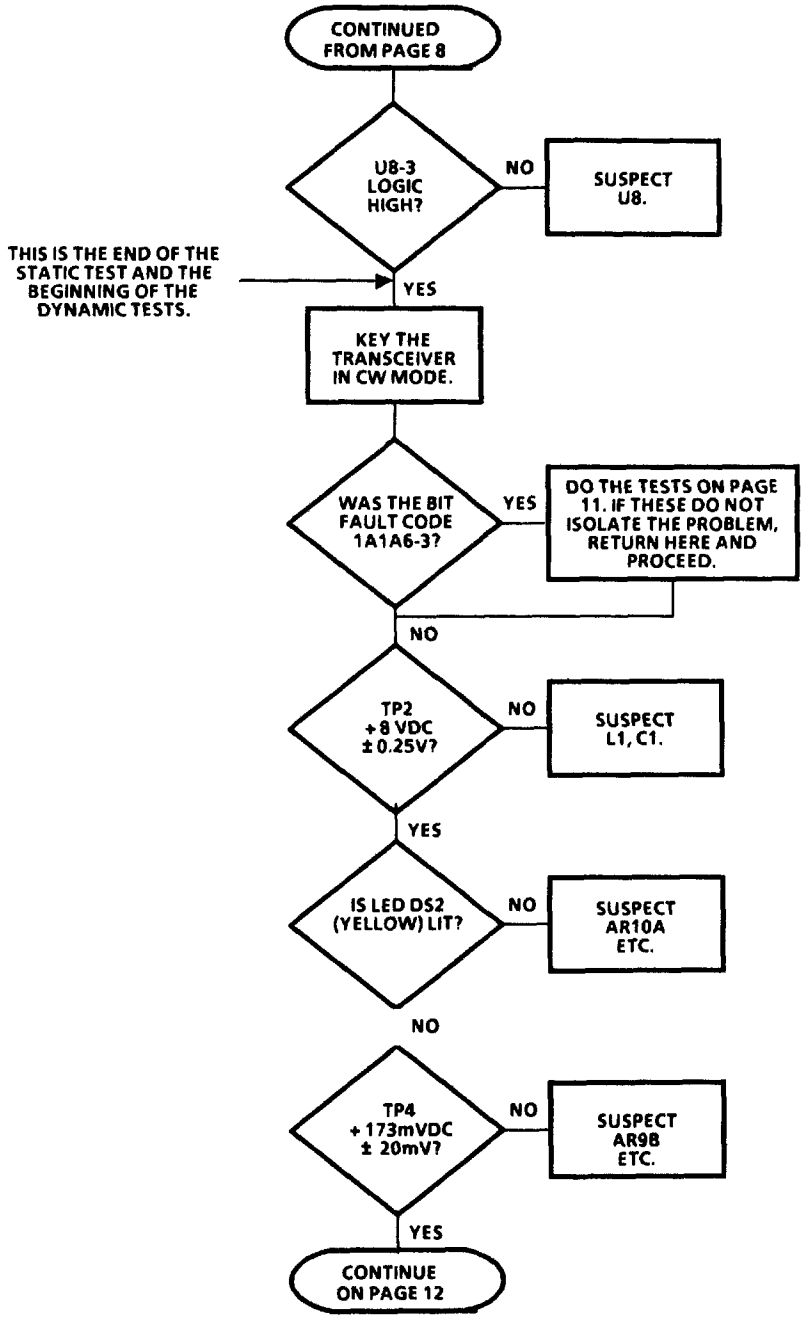


Figure 6-18. TGC Fault Isolation Chart (Page 8 of 15)



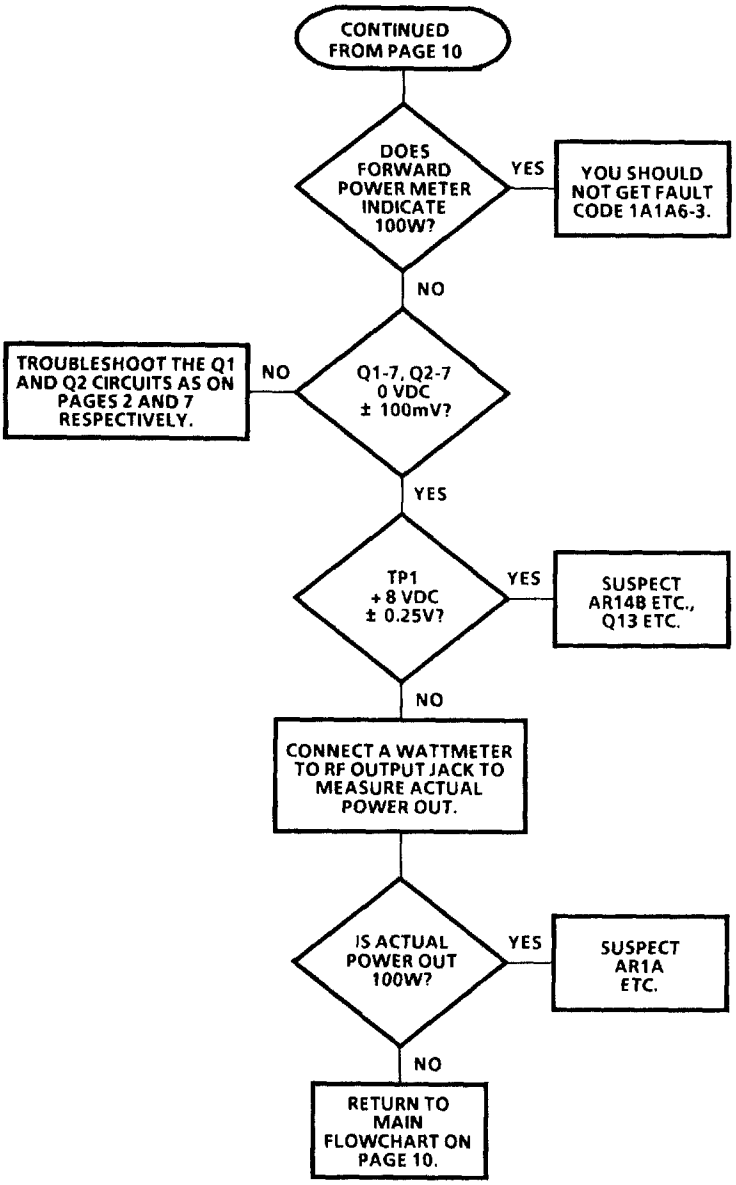
*350-135-9

Figure 6-18. TGC Fault Isolation Chart (Page 9 of 15)



*350-135-10

Figure 6-18. TGC Fault Isolation Chart (Page 10 of 15)



*350-135-11

Figure 6-18. TGC Fault Isolation Chart (Page 11 of 15)

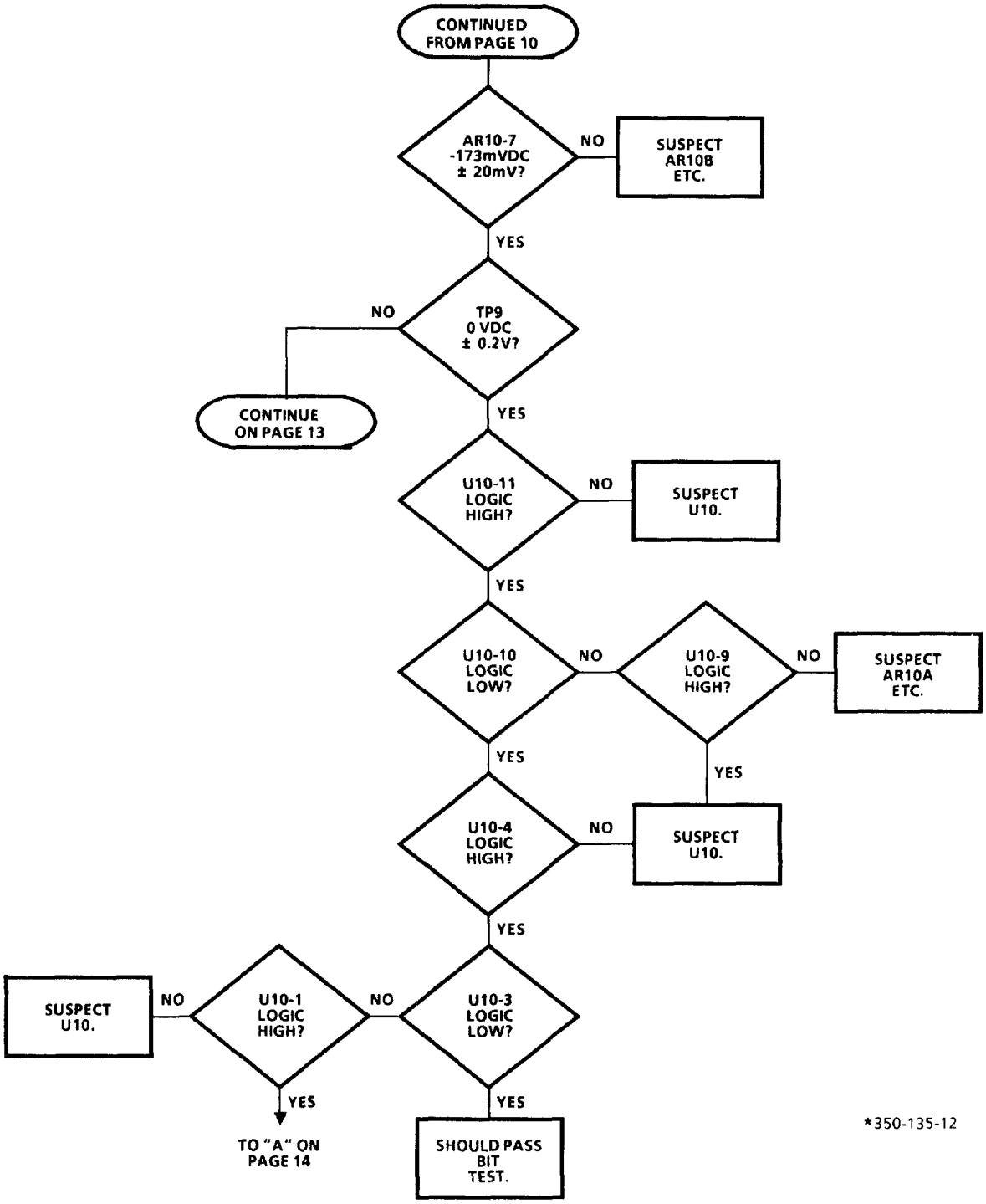
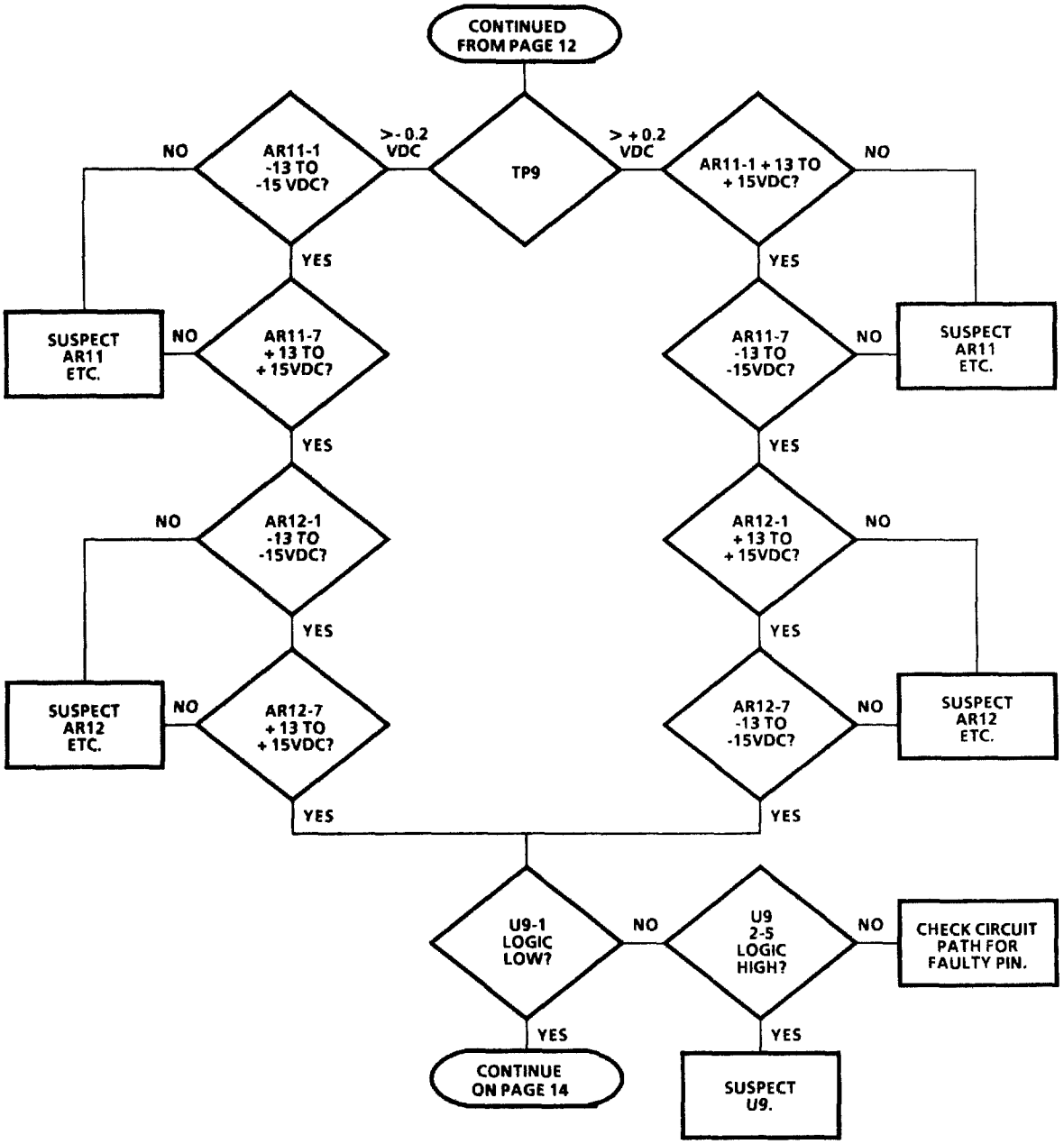
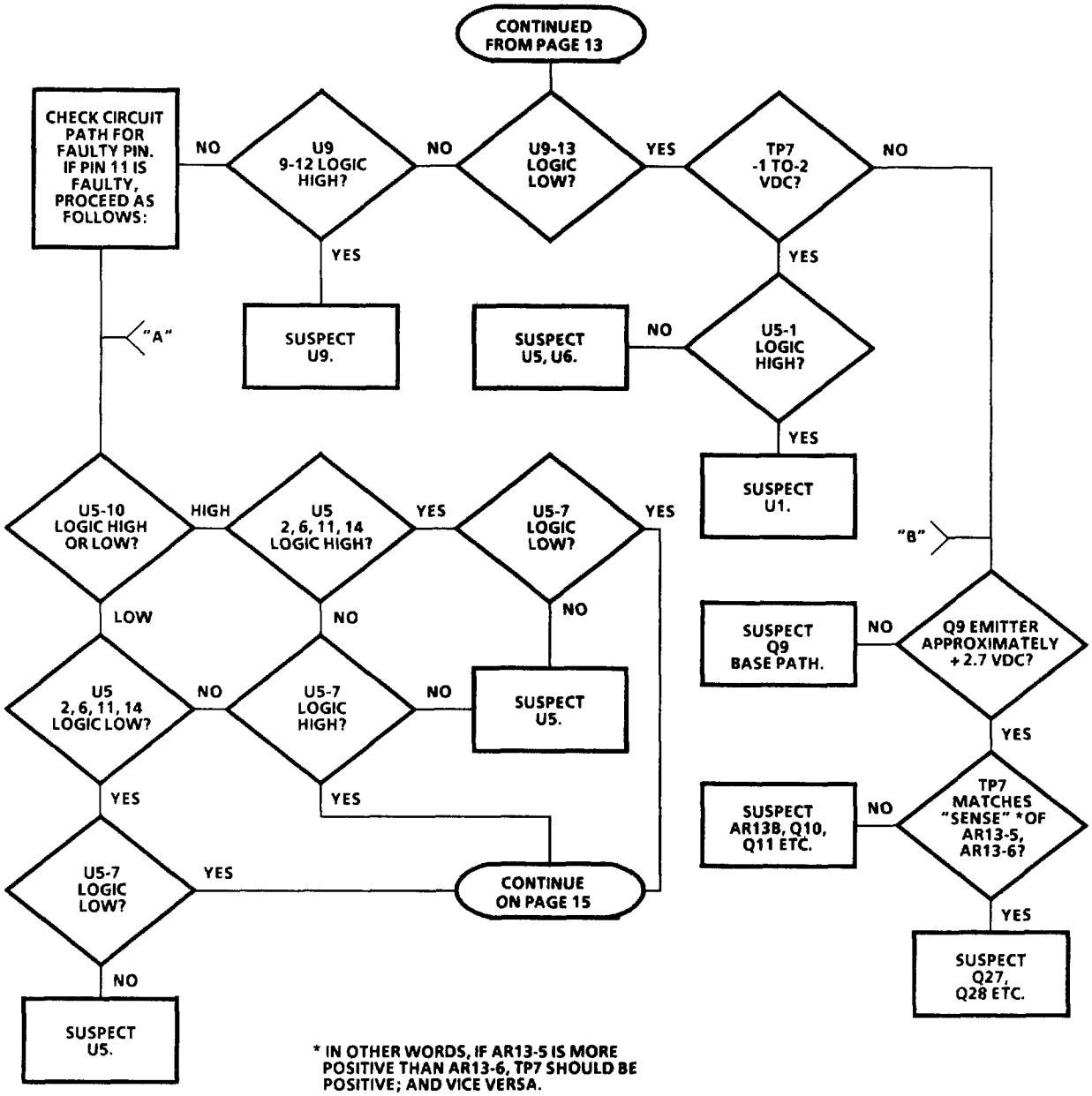


Figure 6-18. TGC Fault Isolation Chart (Page 12 of 15)



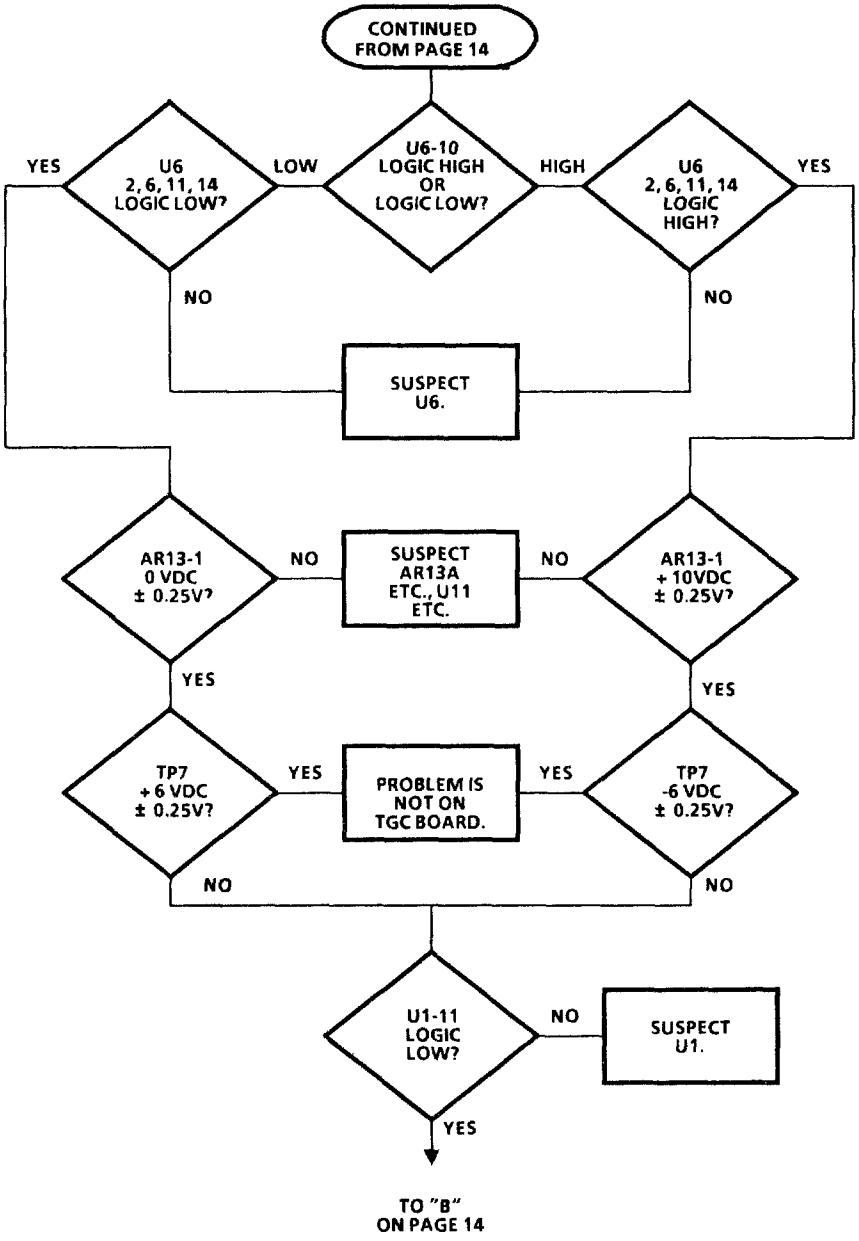
*350-135-13

Figure 6-18. TGC Fault Isolation Chart (Page 13 of 15)



*350-135-14

Figure 6-18. TGC Fault Isolation Chart (Page 14 of 15)



*350-135-15

Figure 6-18. TGC Fault Isolation Chart (Page 15 of 15)

1A1A7-0

This fault code indicates that the microprocessor sent data to the Receiver PWB Assy but did not receive the MCB loop back bit in return.

The fault has to be in the MCB loop back circuitry (U23, U22A, U18, U19, U20, U22E, U22F) or the clock circuitry (U22B, U22D).

(1) Check pin 11 of U19 with an oscilloscope. This pin should go momentarily high (MCB loop back bit) at the beginning of the BIT test.

(2) If not, check U19, U18, U22A, and U23. Check also the RF CLOCK signal (625 KHz) at U22B and U22D.

(3) If the MCB loop back bit is good at pin 11 of U19, check U20, U22F, and U22E.

1A1A7-1

This fault code indicates that the receive 2nd IF signal was not detected at J2 (the output to the IF Filter PWB Assy).

(1) Check the BIT Detector circuit as follows:

(a) Inject a 40.455 MHz signal at -40 dBm into J1.

(b) Connect a spectrum analyzer to J2.

(c) You should see a 455 KHz signal at -36 dBm (or greater).

(d) If the signal is good, then the BIT Detector (Q5, Q6, and their associated components) is bad.

(e) If the signal is bad, proceed to step 2.

(2) Check that CR3 is forward biased and that CR4 is reverse biased. If this is not the case, troubleshoot the pin diode T/R switch circuitry (CR3, CR4, R7, R8, R14, C21, C23). If the diodes are biased correctly, proceed to step 3.

(3) Check the junction of L19 and pin 8 of U1 with an oscilloscope. You should see a 40 MHz signal at least 1 V pk-pk in amplitude. If not, the problem is in the LO Amplifier Q4 and its associated circuitry If the signal is good, proceed to step 4.

(4) Check that CR2 is forward biased by more than 0.5 V and that CR1 is not forward biased by more than 0.4 V. If not, troubleshoot the Attenuator circuit (CR1, CR2, R1, R2, C2, L1, L3, R5, C5, R4, R3, and CR37). If the diodes are correctly biased, proceed to step 5.

(5) The problem is either in the IF Amplifier (Q1 and its associated components) or in the Mixer (U1 and its associated components). Try replacing Q1 and U1 and/or signal tracing (this may be difficult due to the low signal level).

1A1A7-2

This fault code indicates that a low LINE level was detected at the output of AR9A (pin 1).

(1) Troubleshoot the signal path as follows:

(a) Select AME mode on the transceiver front panel.

(b) Select AGC OFF.

(c) Inject a 454 KHz, -80 dBm signal at J5.

(d) Connect an oscilloscope to TP1. You should see a 454 KHz signal at 35 mV pk-pk.

(e) If not, check the biasing of the pin diodes: CR7 should be forward biased, and CR8 should be reverse biased. If the diodes are incorrectly biased, troubleshoot the T/R switch circuitry (CR7, CR8, R10, C38, R31, R9, C39). If the diodes are correctly biased, troubleshoot the IF Amplifier (Q8-Q11).

(f) If the signal at TP1 is good, proceed to step 2.

(2) Select USB on the transceiver front panel and do the following:

(a) Connect the oscilloscope to TP2. You should see a 1 KHz audio signal at an amplitude of 200-400 mV pk-pk.

(b) If not, check the collector (case) of Q13 with the oscilloscope. You should see a 455 KHz signal at approximately 4.4 V pk-pk. If this signal is bad, the BFO Amplifier (Q7, Q13, and their associated components) is at fault.

(c) If the signal at Q13 is good, the problem is in the Buffer Amplifier (Q12 and its surrounding circuitry), Mixer U2, or the Audio Amplifier (AR1 and its associated components).

(3) If TP2 is good, do the following:

(a) Check the audio signal at pin 4 of U4 with the oscilloscope. It should be the same as at TP2.

(b) If not, U4 is probably bad.

(c) Check for the same audio signal at pin 15 of U5. If it is not there, U15 or its associated circuitry is probably bad.

(d) If the signal is good at U15, then the problem is in AR3B or AR9.

NOTE

When troubleshooting this area, make sure that the front panel LINE potentiometer is not set for minimum output. Otherwise, you won't get any signal indication.

1A1A7-3

This fault code indicates that the pin diode T/R switch (CR3, CR4) at the J2 output is faulty.

(1) Put the transceiver in the transmit mode with the 2ND, TX KEY buttons on the front panel.

(2) Check the biasing of CR3 and CR4: CR3 should be reverse biased, and CR4 should be forward biased. If not, check the diodes and their associated components (R8, C23, C21, R7, R14).

(3) If the diodes are correctly biased, the problem has to be a bad connector (J3) or a bad circuit board trace.

1A1A7-4

This fault code indicates that there is a problem with the AGC voltage. Since we can assume that our AGC/TGC PWB Assy is good and that our Receiver PWB Assy is bad, the problem has to be in either the AM Detector (where the AGC voltage originates) or the two AGC attenuators (CR1, CR2 or CR9-CR11).

(1) Check the AM Detector as follows:

(a) Select AGC OFF on the transceiver front panel.

(b) Inject a 454 KHz, -80 dBm signal at J5.

(c) Check the junction of R85 and the emitter of Q16 with a DC voltmeter. You should see approximately +0.25 Vdc.

(d) Increase the output of the signal generator to -74 dBm.

(e) Check the voltage at the emitter of Q16 again. It should have increased to +0.5 Vdc.

(f) If the voltage in either case is bad, the problem is in the AM Detector (Q14-Q16 and their associated components).

(2) If the voltages at Q16 are good, then the problem is in one of the AGC attenuators: CR1, CR2, and their associated components; or CR9-CR11 and their associated components.

1A1A1-2

This fault code indicates that the pin diode T/R switch (CR7, CR8) at the J5 input is faulty.

(1) Put the transceiver in the transmit mode with the 2ND, TX KEY buttons on the front panel.

(2) Check the biasing of CR7 and CR8: CR7 should be reverse biased, and CR8 should be forward biased. If not, check the diodes and their associated components (R10, C38, R31, R9, C39).

(3) If the diodes are correctly biased, the problem has to be a bad connector (J6) or a bad circuit board trace.

1A1A6-2

This fault code indicates that one of the AGC attenuators is not functioning properly.

Check the CR1, CR2 AGC Attenuator and its associated components (C2, L1, R2, L3, R1, R5, C5, R4, CR37, R3) and the CR9-CR11 AGC Attenuator and its associated components (C42, R32, R37, C44, R197, C48, R47, C53, R51).

ADDITIONAL SYMPTOMS

The above fault codes cover the main signal path, but there are several other circuits on the Receiver PWB Assy that could cause problems. However, these circuits are readily identified by the following obvious symptoms:

No Sidetone

Check AR2B, U4A, and their associated components.

Bad PATCH Audio Output

Check AR10B and its associated components.

Bad NBSV Audio Output

Check AR10A, Q25, and their associated components.

No Speaker Audio

Check AR11, U5C, and their associated components.

No Headphone Audio

Check AR8B and its associated components.

No Speaker or Headphone Audio

Check U5A, AR12A,and their associated components. There could also be a problem in the squelch circuitry, which causes U5A to open the audio line to the speaker and headphone.

Incorrect SQUELCH Operation

Check the operation of the SQUELCH circuitry as follows:

(1) Connect an RF signal generator to the antenna jack (J1) at the rear of the transceiver.

(2) Select LSB on the transceiver at a frequency of 5 MHz.

(3) Set the signal generator carrier frequency to 4.999 MHz at -20 dBm.

(4) Manually adjust the SQUELCH control on the transceiver front panel, and check to see that the speaker audio is squelched as you rotate the control clockwise. Adjust the control so that the audio just squelches.

(5) Modulate the carrier frequency with a 20 Hz signal at 50% modulation.

(6) The squelch should break.

If the SQUELCH circuitry does not respond as described above, do the following:

(7) Leaving the signal generator set up as before (with 50% modulation), connect a DC voltmeter to pin 2 of AR6A. You should see a positive DC voltage which varies in proportion to the increase or decrease in the percentage of modulation on the signal generator. If the voltage here is good, skip to step 9. If not, continue with step 8.

(8) Check the base of Q20 for a 1 KHz audio signal modulated at 20 Hz. If the signal is not good there, the problem is in the Audio Compressor circuit (AR4A, Q19, Q20, and their associated components). If the signal

is good, check for a 20 Hz audio signal at the output of the Bandpass Filter, AR5A pin 1. If this signal is not good, the problem is in the Rectifier (AR4B and its associated components) or the Bandpass Filter (AR5A and its associated components). If the signal is good at AR5A pin 1, then the problem is in rectifier AR5B or its associated components.

(9) Check the inputs to Comparator AR6B, pins 5 and 6. The voltage at pin 5 is determined by the setting of the SQUELCH control. With a DC voltmeter, check that this voltage varies as you adjust the SQUELCH control. The voltage on pin 6 should vary as you adjust the percentage of modulation on the signal generator. If it does not, DC Amplifier AR6A (or its associated components) is probably bad. When the voltage at pin 6 becomes more positive than the voltage at pin 5, then the output at pin 7 should go low. This is the unsquelched condition. When the voltage at pin 5 is more positive than at pin 6, pin 7 should go high. This is the squelched condition. If the output at pin 7 does not behave as described, then the problem is in AR6B.

(10) If the output of Comparator AR6B is good, then the problem has to be in the diodes CR19, CR20, or in Buffer Amplifier AR7B (or their associated components). You can also check the SQUELCH MONITOR line at pin 11 of switch U5A. This line should be low during the unsquelched condition and high during the squelched condition.

6-12. CRYSTAL OSCILLATOR ASSEMBLY, A1A8. There is no troubleshooting procedure for the Crystal Oscillator Assembly. The purpose of the following procedures is (1) to determine whether the Crystal Oscillator Assembly is functioning properly; and, if it is found to be off-frequency, (2) to attempt to adjust the frequency to the specified value.

a. Output Check.

(1) Disconnect the power cable for the Crystal Oscillator Assembly in the test-bed transceiver (this cable plugs into J12 on the Interconnect PWB Assy). In its place, connect the power cable for the Crystal Oscillator Assembly you are testing. It is not necessary to mount this Crystal Oscillator Assembly in the transceiver.

(2) Turn on the transceiver, and check the supply voltages at pins E1, E2, and E3 of the Crystal Oscillator Assembly. These voltages should be within 0.5 V of the nominal value.

E1, +15 Vdc
E2, 0 Vdc
E3, +13.6 Vdc

(3) Obtain an SMB female to BNC adapter cable of 18 inches (or less) in length. Connect the SMB female end to the Crystal Oscillator Assembly, and connect the BNC end to an oscilloscope.

(4) Check for a 10 MHz sine wave on the oscilloscope with an amplitude of 0.6 to 1.0 V pk-pk.

(5) If you do not get this signal, the Crystal Oscillator Assembly is defective and should be discarded. If the signal looks good, proceed to the frequency check below.

b. Frequency Check.

(1) Disconnect the adapter cable from the oscilloscope, and connect it to a frequency counter. The frequency counter should be referenced to a frequency source whose stability is better than 1 part in 10 per day.

(2) Check that the frequency of the Crystal Oscillator Assembly is 10.000000 (+/- the offset, if specified on the label) MHz.

NOTE

Some Crystal Oscillator Assemblies may have an offset. The reason for this offset is to enable the Crystal Oscillator Assembly to meet the temperature stability specification, which demands that the frequency not vary more than 3.3 Hz from the nominal value over the entire temperature range (-30 to +75 C). For example, the Crystal Oscillator Assembly may have to be set for a room-temperature (25 C) frequency of 10.000001 MHz in order to meet

the temperature stability specification. In this case, the offset would be +1 Hz.

(3) If the frequency is not correct, do the adjustment procedure for the Crystal Oscillator Assembly (see Section II, Alignment Procedures).

6-13. REFERENCE/BFO PWB ASSY, A1A9.

a. Preliminary Procedure.

(1) Remove the good Reference/BFO PWB Assy from the test-bed 100 Watt Transceiver, and replace it with the faulty R eference/BFO PWB Assy.

(2) Power up the transceiver.

(3 Connect a dummy load to the transceiver.

(4) Check for the presence of the following power supply voltages on the board:

Voltage:	Measure at:
+5 V-A	+ side of C82
+5 V-B	+ side of C83
+5 V-C	+ side of C65
+15 V	+ side of C66

(5) If the voltages check good, run the receive-transmit BIT test.

b. Interpreting the BIT Fault Codes. Use the fault codes listed below as a guide in troubleshooting the Reference/BFO PWB Assy. Refer to the section corresponding to the fault code you get. In the event that the test runs without generating a fault code, start at the beginning of the following procedures and work your way through to the end.

BIT Test Description for the Reference/BFO PWB Assy

1. Verifies the presence of the 1 KHz, 455 KHz (nominal), and 40 MHz outputs from the board.

2. Verifies the frequency lock of the BFO at both ends of the frequency range.

NOTE

If the BFO is out of lock, the FAULT light on the transceiver front panel illuminates. This happens independently of the BIT test. For this reason, BFO unlock is referred to as a "run-time fault," since the BIT test does not have to be run for the FAULT light to come on.

1A1A9-1
FAULT light illuminates without BIT
(run-time fault)

In this case, the FAULT light came on as soon as the transceiver was powered up (and before the BIT test was run). Therefore, this fault code indicates that there is a problem in the phase lock loop circuitry.

(1) Check to see whether the BFO is really out of lock as follows:

(a) Check for a low at the collector of Q9, which is the RF ATTN line. If Q9's collector is low, which it should be during a BFO unlock condition, then the collector of Q7 should be high.

(b) If the collector of Q7 is not high, then look for a problem in the Q9 area (possible Q9 collector-to- emitter short, for example).

(c) If the collector of Q9 is low and the collector of Q7 is high, connect a frequency counter to the junction of R58 and R59. (To access R58 and R59, you must remove the shield from the VCO Assembly.)

(d) Center-tune the BFO by going to USB or LSB receive mode and leaving the BFO key on the transceiver front panel deactivated.

(e) The frequency displayed on the frequency counter should be 45.500 MHz. If it is not, the BFO is unlocked; and the problem is in the phase lock loop circuitry. Proceed to step 2.

(2) Check the phase lock loop circuitry as follows:

(a) If you have not already done so, remove the shield from the VCO on the Reference/BFO PWB Assy.

(b) Look at TP2 with an oscilloscope. You should see a positive DC voltage (at 6.5 Vdc) with no AC component. If TP2 is good, skip to step 3. If not, proceed to step c.

(c) If TP2 is bad, check the VO and RO outputs of U5 (pins 8 and 7, respectively).

i. In the locked condition (when the reference frequency = the variable frequency), VO and RO should be logic high with a series of low-going pulses (approximately 1 us wide) spaced 1 ms apart.

ii. In the unlocked condition (when the reference frequency is either higher or lower than the variable frequency), both VO and RO should be square waves. These square waves will be approximately opposite to each other; that is, when VO is negative, RO is positive and vice versa.

(d) Connect a voltmeter to TP1. If RO is low more than it is high, the voltage at TP1 should approach the +15 V supply. If VO is low more than it is high, the voltage at TP1 should approach 0. (In the locked condition, TP1 should be approximately +6.5 Vdc.)

(e) If the voltage at TP1 is in accord with the VO and RO signals at the output of U5, proceed to step 3. If not, trace the VO and RO signals through U6 and Q11-Q13.

(3) Check the VCO as follows:

(a) Center-tune the BFO (see step 1d above).

(b) Unsolder one end of R54.

(c) Connect the positive lead of a DC power supply to TP2 and the negative lead to the VCO shield.

(d) Connect a frequency counter to the junction of R58 and R59.

(e) Adjust the power supply for +4 Vdc at TP2. The frequency counter should read approximately 40 MHz.

(f) Increase the voltage to 6.5. The frequency counter should now read 45.5 MHz.

(g) Increase the voltage to 9.6. The frequency counter should read approximately 50 MHz.

(h) If the VCO performs as described above, proceed to step 4. If not, decrease the power supply voltage to 6.5 and adjust C35 for 45.500 MHz on the frequency counter. Then repeat steps e-h. If the VCO still does not function correctly, troubleshoot the internal VCO circuitry.

(4) Check the inputs to U5 as follows:

(a) Adjust the power supply output to 6.5 Vdc, and verify that the output frequency of the VCO is 45.500 MHz. Connect the frequency counter to pin 12 of U8 (or pin 1 of U5), and check for a frequency of 910 KHz. Replace the frequency counter with an oscilloscope, and check for a TTL (0-5 V) square wave with a 20% duty cycle (signal should be high 20% of the time). If the signal is good, proceed to step b. If not, trace the signal back through U8-2 (4.55 MHz), U7-15 (45.5 MHz), and the source of Q15 (45.5 MHz).

(b) Check for an 8 KHz TTL square wave at pin 27 of U5. If this signal is good, replace U5. If not, trace the 8 KHz line back to U12.

1A1A9-1

FAULT light does not illuminate until BIT test is run.

Since the FAULT light did not illuminate until after the BIT test was run, this fault code indicates that the phase lock loop circuitry is working properly. The problem is that one of the three output frequencies (1 KHz, 455 KHz, or 40 MHz) is incorrect or missing.

The first thing to do is check the BIT Detector circuit as follows:

(1) Verify that the collector of Q8 is low (this is the fault condition).

(2) Check the voltage on the base of Q6. Under normal conditions (no fault), the voltage here should be the same as on the emitter (+5 Vdc), indicating that Q6 is not conducting. If this is the case, then the problem is in the BIT Detector (Q6, Q5, and their associated components).

(3) If Q6 is biased to conduct (base voltage is less than the emitter voltage), then check the cathodes of CR17, CR23, and CR27 to determine which of these diodes is conducting. Once you know which of these diodes is on, you know which circuit to troubleshoot:

Conducting diode:	Faulty circuit:
CR17	40 MHz
CR23	455 KHz (BFO/Carrier)
CR27	1 KHz

Refer to the appropriate troubleshooting section below.

40 MHz

(1) Check the gate (case) of Q3 for a 40 MHz sine wave at 1.2 V pk-pk. If the signal here is good, then the problem is in the BIT Detector (Q3, Q4, and their associated components). If the signal here is the correct frequency but low, you might try adjusting L1 and L2 to get more output. Refer to the alignments section.

(2) If the signal at the gate of Q3 is bad, check pin 3 of U14 for a 10 MHz TTL (0-5 Vdc) square wave. If this signal is bad, then the problem is probably U14 (since the circuitry prior to U14 is common to the other two frequency outputs, which we know are good).

(3) If the signal at pin 3 of U14 is good, the problem is in the multiplier circuitry (Q1, Q2, and their associated components). Check the collector of Q2 (not the case) for a distorted 40 MHz sine wave (the sine wave should be "ringing" at a 10 MHz rate) at 4.5 V pk-pk (maximum), and work your way backwards or forwards from this point.

455 KHz (BFO/Carrier)

NOTE

The BFO/Carrier BIT amplifier (Q19) is normally off. It is turned on only during the BIT test.

(1) Check the gate (case) of Q18 for a 455 KHz (+/- 1 KHz) sine wave at 1 V pk-pk. If the signal here is good, the problem is in the BIT Detector (Q18, Q19, and their associated components).

(2) If the signal at the gate of Q18 is bad, check the collector of Q17 for a 455 KHz (+/- 1 KHz) square wave at 0-5 V pk-pk. If the signal here is good, the problem is in the 455 KHz Filter (C47-C53 and L6). If not, proceed to step 3.

(3) Check for a TTL (0-5 Vdc) square wave at the output of U9 (pin 2). If the signal is bad here, check for a sine wave at the input (pin 7). If the input is good, replace U9. (The input to U9 should be good. Otherwise, the BFO would be out of lock, since the same signal is applied to the phase lock loop circuitry.)

1 KHz

(1) Check pin 1 of AR1 for a 1 KHz sine wave at 4.2 V pk-pk. If the signal here is good, then the problem is probably in the 1 KHz BIT Detector (Q10 and its associated components). To verify this, check the

collector of Q10. The voltage here should be within 0.2 to 0.4 V of the emitter voltage.

(2) If the signal at AR1 pin 1 is bad, check at E2 for a 1 KHz TTL (0-5 Vdc) square wave. If the signal is good here, the 1 KHz Filter (AR1 and its associated components) is probably bad.

(3) If the signal is bad at E2, verify that a 200 KHz TTL square wave is coming out of U11 pin 3. (U11 should be good, since the 200 KHz reference to the Synthesizer originates here. If this signal was absent, fault code 1A1A10-1 would be declared.) Then trace the signal through U12 and U13, noting that its frequency gets divided down in successive stages until it becomes 1 KHz at pin 9 of U13.

1A1A10-1
FAULT light illuminates without BIT
(run-time fault)

This fault code indicates that there is a problem with the 200 KHz reference signal originating on the Reference/BFO PWB Assy, since without this the Synthesizer cannot lock (which is the reason why a Synthesizer fault code is displayed).

(1) Check the output of P2 on the Reference/BFO PWB Assy for a 200 KHz TTL (0-5 Vdc) square wave.

(2) Work your way back through U11, U14, Q22, and Q21, all the way to the 10 MHz input from the Crystal Oscillator Assembly at J2 (the signal level here should be a 10 MHz sine wave at 0.5 to 1 V pk-pk). The signal level at the source of Q21 should be a little less than at J2, and the signal at the collector of Q22B should be the 10 MHz TTL (0-5 Vdc) square wave (the signal is changed from a sine wave to a square wave in Q22).

6-14. SYNTHESIZER PWB ASSY, A1A10.

a. Preliminary Procedure.

(1) Remove the good Synthesizer PWB Assy from the test-bed 100 Watt Transceiver, and replace it with the faulty Synthesizer PWB Assy.

(2) Power up the transceiver.

(3) Check for the presence of the following power supply voltages on the board. Voltages should be within 0.5 V of the nominal value.

Voltage:	Measure at:
+15 V-A	+ side of C2
+15 V-B	+ side of C63
+5 V-A	+ side of C6
+5 V-B	+ side of C67
-15 Vdc	- side of C72

(4) If the voltages check good, run the receive-only BIT test. Refer to the section corresponding to the fault code you get.

b. Interpreting the BIT Fault Codes. Use the fault codes listed below as a guide in troubleshooting the Synthesizer PWB Assy. In the event that the test runs without generating a fault code, start at the beginning of the following procedures and work your way through to the end.

BIT Test Description for
the Synthesizer PWB Assy

1 - Verifies the presence of the Synthesizer PWB Assy by sending data to it and receiving data back.

2 - Verifies the presence of the Synthesizer output and frequency lock at both ends of the tuning range.

1A1A10-0

This fault code indicates that the microprocessor did not receive a response (the MCB loopback bit) when it sent data to the Synthesizer PWB Assy.

(1) Check the cable going to J3 on the Synthesizer PWB Assy.

(2) Connect an oscilloscope to pin 11 of U7 (this is where the MCB loopback bit originates).

(3) Run the receive-only BIT test and verify that pin 11 of 7 changes state. This change of state is the MCB loopback bit which is fed on the RF DATA line via U2 and U3 to pin 10 of J3 and from there back to the microprocessor.

(4) If no change of state occurs, check the data, clock, and strobe lines into U5, U6, and U7.

NOTE

The strobe pulse may be very difficult to see without a storage scope. At the inputs to shift registers U5, U6, and U7, the strobe pulse is a positive-going signal of 1.5 to 2.0 usec in width; at the input (pin 1) and output (pin 15) of U1, the strobe pulse is a negative-going signal, which is inverted by Q45 before being applied to U5, U6, and U7. The strobe signal is what causes pin 11 of U7 to change state after all the data bits have been clocked into U5, U6, and U7.

1A1A10-1

This fault code indicates that the Synthesizer is out of lock.

(1) Disconnect the coax cable from J5 on the First Converter PWB Assy (this cable originates at P1 on the VCO), and connect it to the RF input of the spectrum analyzer.

(2) Adjust the spectrum analyzer to scan from 0 to 110 MHz, with the top vertical line on the analyzer display equal to +10 dBm.

(3) Set the test-bed transceiver for USB at a frequency of 1.64500 MHz. (This sets the Synthesizer frequency to 42.10000 Mhz.)

(4) Connect the oscilloscope to TP3 on the Synthesizer PWB Assy. If the Synthesizer is operating properly, the voltage on TP3 should be +8.2 +/- 0.4 Vdc with no AC component.

(5) While observing the voltage on TP3, also observe the spectrum analyzer display.

Case 1: The Synthesizer frequency is less than 35 MHz, and the voltage on TP3 is greater than +11.5 Vdc.

Conclusion: The VCO is probably okay. The problem is most likely in the reference frequency signal path.

Procedure: Check for a 100 KHz signal (pulses) at pin 11 (or pin 5) of U19. If the signal is not there, work your way back through Q4 and U17A, which divides the 200 KHz reference coming in from J1.

Case 2: The Synthesizer frequency is greater than 70 MHz, and the voltage on TP3 is greater (more negative) than -6 Vdc.

Conclusion: The VCO may or may not contain the fault.

Procedure:
1. Check the VCO. See the procedure below.
2. Check the Sample and Hold circuitry. See the procedure below.
3. Check the Divide by N circuitry. See the procedure below.
4. Check the Integrator circuitry. See the procedure below.

SAMPLE AND HOLD
Checkout Procedure

1. Quick Check:

(a) Observe the voltage waveform on TP2. In a properly working Synthesizer, the waveform should appear as on page 7 of the schematic diagram.

(b) If TP2 indicates a pure DC level greater than +11.5 Vdc, and if TP3 is the same, then the Sample and Hold circuitry is probably okay.

(c) Similarly, if TP2 indicates a pure DC level greater (more negative) than -6 Vdc, and if TP3 is the same, then the Sample and Hold circuitry is probably okay.

(d) If neither (b) nor (c) is true, then perform the Detailed Checkout Procedure below.

2. Detailed Checkout Procedure:

(a) With an oscilloscope, check the voltage at pin 3 of AR2. This voltage should be the same as on pin 6, which is the same as TP3.

(b) Check the voltage on pin 2 of AR2, which should be the same as the voltage on pins 3 and 6.

(c) Check pin 11 of U5 for the SAMPLE CONTROL signal, which should be a series of positive pulses 280-500 ns wide at a frequency of 100 KHz (when the Synthesizer is in lock).

(d) Remove P1 from J7 and P2 from J8. This isolates the Sample and Hold circuitry.

(e) Connect a DC power supply to the circuit as follows: + lead to J7-2 (the pin closer to the VCO) and - lead to TP4 (GND).

(f) Connect the oscilloscope to TP3.

(g) Vary the power supply voltage from 0 to 10 Vdc. The waveform on TP3 should be a positive DC equal to the power supply voltage.

(h) Reverse the polarity of the power supply (+ lead to TP4 and - lead to J7-2).

(i) Vary the voltage as before. The voltage on TP3 should be a negative DC equal to the power supply voltage.

(j) If the SAMPLE CONTROL signal is good, but the Sample and Hold circuit does not respond properly to the power supply voltage, the problem has to be in transistors Q20-Q27, op amp AR2, or their associated components.

VCO OSCILLATOR AND AMPLIFIER
Checkout Procedure

1. Quick Check:

A quick and easy way to determine whether the VCO is the cause of a Synthesizer unlock condition is to substitute a known good VCO board for the one in the Synthesizer you are troubleshooting. If the Synthesizer functions correctly with the substitute VCO, then the original VCO is faulty; if not, then the problem is somewhere other than in the VCO.

2. Detailed Checkout Procedure:

(a) Remove jumper plug P2 from J8 on the Synthesizer PWB Assy.

(b) Remove jumper plug P3 from J5.

(c) Connect an RF voltmeter with a 50-ohm probe across pins 3 and 1 (GND) of J5.

(d) Disconnect the VCO output cable P1 from J5 on the First Converter PWB Assy. Using an SMB to BNC adapter, connect this cable to the input of a frequency counter.

(e) Connect the + lead of a DC power supply to J8-2 (pin 2 is the one closer to the VCO), and connect the - lead to TP4 (GND).

(f) Adjust the power supply for 8.2 Vdc. The frequency counter should read 42.10 +/- 2.1 MHz. The reading on the RF voltmeter should be 50 mV rms or greater.

(g) Reverse the polarity of the power supply leads.

(h) Adjust the power supply for 7.0 Vdc. The frequency counter reading should be greater than 70 MHz, and the RF voltmeter should indicate 50 mV rms or greater.

(i) Disconnect the RF voltmeter.

(j) Disconnect the VCO cable from the frequency counter, and connect it to the 50-ohm probe of the RF voltmeter.

(k) The reading on the voltmeter should be between 0.45 V rms and 0.16 V rms as the power supply voltage is varied from 0 Vdc to 7 Vdc.

DIVIDE BY N
Checkout Procedure

(a) Remove jumper plug P3 from J5 on the Synthesizer PWB Assy.

(b) Connect a coaxial test cable (Pomona Electronics 3787- C-36 or equivalent) to pins 1 (GND) and 2 of J5. Connect the BNC end of the test cable to the output jack on the rf signal generator.

(c) Set the output frequency of the signal generator to 42.10000 MHz, and set the output level to -10 dBm.

(d) Set the frequency of the test-bed transceiver to 1.64500 MHz, and set the mode to USB.

(e) Connect a 24-pin DIP clip to U5, a 16-pin DIP clip to U15, and a 14-pin DIP clip to U14.

(f) Connect a x10 oscilloscope probe to the 1 megohm input of a frequency counter.

(g) Check the following pins with the oscilloscope probe:

U5-2
U5-11
U14-9
U15-2
U15-7
U15-10
U15-12
U15-15

Each pin should have a frequency of 100.0 KHz.

(h) Connect the x10 probe to an oscilloscope and monitor the waveform at U19-6. The waveform should be a series of extremely narrow pulses with a frequency of 100 KHz. The peak of the pulse should be greater than +4.0 Vdc, and the low level should be +3.3 Vdc or less.

(i) Connect the probe to U19-11. This waveform should have the same characteristics as the one in the previous step.

INTEGRATOR
Checkout and Troubleshooting Procedure

1. Checkout:

(a) Set up the oscilloscope for two-channel operation.

(b) Connect the probe for Channel 1 to TP2, which is the output of the Integrator.

(c) Connect the probe for Channel 2 to the cathode of CR12, where you should see the DELAYED BIAS signal (refer to the Synthesizer Integrator Timing Diagram on figure FO-7 of the On-Equipment Manual, T.O. 31R2-2URC-81.)

(d) As shown on the timing diagram, the voltage at TP2 should start to ramp down when the DELAYED BIAS signal goes high.

2. Troubleshooting:

We will consider the following two cases:

<u>Case 1</u>

The Integrator does not ramp down. The Integrator output is a steady DC voltage greater than +11.5.

(a) Check the DELAYED BIAS signal at the cathode of CR12. This signal should go positive, as shown in the timing diagram FO-7 in the On-Equipment Manual,

T.O. 31R2-2URC-81. If not, the problem is in the DELAYED BIAS circuitry. Check the following:

U15-3 (DELAYED BIAS)
U15-2 (BIAS - should be one clock pulse (about 0.2 us) ahead of DELAYED BIAS)
U5-9 (BIAS)
U5-2 (CYCLE START - 100 KHz)
U5-8 (VCO frequency/10)

If U5-2 and U5-8 are good, but U5-9 is bad, check the power supply pins of U5: U5-24 = +5 Vdc; U5-12 = 0 Vdc. Also check U5-17 (RESET), which is normally high. If these pins are all okay, replace U5.

(b) Check the ramp-down current source as follows:

Q16, drain (should be a square wave, high for approximately 3.5 us, from -1.35 V to +0.4 V)
Q16, source (+5 +/- 0.25 Vdc)
Q19, source (+8.8 +/- 0.2 Vdc)

If the three voltages above are good, the problem is probably in the discrete-component op amp.

Case 2

The Integrator output at TP2 is saturated at the negative DC supply voltage; i.e., greater (more negative) than -11.5 Vdc.

Connect the Channel 1 oscilloscope probe to TP2. Connect the Channel 2 oscilloscope probe to TP1. When TP1 goes negative to approximately -1.2 Vdc, the voltage at TP2 should start to ramp down as shown on page 7 of the Synthesizer schematic.

(a) If TP1 does not go negative to -1.2 Vdc, then the problem is most likely between flip-flop U19 and TP1. With the oscilloscope, verify the signals at the following locations:

U19-2 (output, 100 KHz)
U19-3 (output, 100 KHz)
U19-6 (input, 100 KHz)
U19-11 (input, 100 KHz)

Verify the following power supply connections:

U19-1, -16 (+5 Vdc)
U19-8 (0 Vdc)

If the outputs of U19 are bad and all else is good, replace U19. If the outputs of U19 are good, the problem is between U19 and TP1.

(b) If TP1 does go negative to -1.2 Vdc but the ramp (TP2) does not go up, then do the following:

While keeping one channel of the oscilloscope connected to TP2, check the waveform at the cathodes of CR3 and CR4 (refer to figure 6-19).

If the waveform is good, check the ramp-up current sink as follows:

- Check the voltage at the gate (case) of Q11. This is the DELAYED BIAS signal voltage. For the ramp to go up, this voltage must be a low (Q11 not conducting).

- If the gate of Q11 is high, check the DELAYED BIAS signal line from the collector of Q10 to U15-2 and back further if necessary (as in Case 1 above).

- f the DELAYED BIAS signal line is okay, check the gate (case) of Q13, which should have a voltage of -6.2 Vdc with no AC component.

- If this voltage is okay, check the voltage on U21- 15, which should be -8.8 Vdc with no AC component.

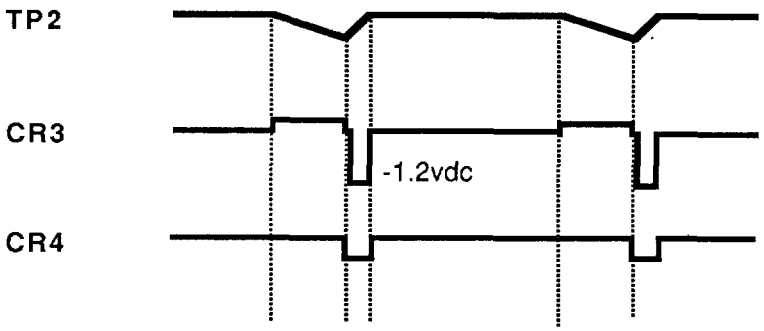


Figure 6-19. TP2 and the Cathodes of CR3, CR4

If none of the above voltages is bad, the problem is most likely inside the discrete-component op amp.

6-15. FRONT PANEL PWB ASSY, A1A11A1.

a. Preliminary Procedure.

(1) You can check all the adjustment potentiometers and the speaker on/off switch without applying power to the Front Panel PWB Assy. If you don't know what the specific problem with the board is, begin by doing this.

(2) Remove the good Front Panel Assembly (which consists of the Front Panel PWB Assy and the Display Assembly) from the test-bed 100 Watt Transceiver, and replace it with the faulty Front Panel PWB Assy. Remove the good Display Assembly from the test-bed Front Panel Assembly and attach it to the faulty Front Panel PWB Assy.

(3) Power up the transceiver.

(4) Check for the presence of the following power supply voltages on the board:

Voltage:	Measure at:
+5 Vdc	+ side of C2
+15 Vdc	+ side of C12
+12 Vdc	+ side of C13
+13.6 Vdc	+ side of C20

(5) If the voltages check good, proceed to the next section, "Troubleshooting Procedures."

b. Troubleshooting Procedures.

(1) If the Display Assembly is installed, check to see whether the backlights are functioning. If they are not, there is a problem with Inverter U8. Check for +13.6 V at the input terminals of the Inverter and 115 Vac 400 Hz at the output terminals.

(2) If the Display Assembly is installed, check to see whether the outline of previous segments persists when you change the segmental pattern by hitting a key. For example, when you change a particular digit from a "3" to a "1" and you can still see the outline of the "3," this indicates that there is a fault in the 60 Hz Oscillator, which consists of U5, R4, R5, and C10.

(3) Check the operation of the FAULT LED DS1 by running the receive-only BIT test. The FAULT LED should come on when you run the test.

(4) Troubleshoot the data path as follows:

(a) Press a key and check the bit pattern on pins 3, 4, and 11-14 on U4. Hit a different key and check the bit pattern again. The pattern should change every time you press a different key. If this is the case, then U2, U3D, and U9B are probably good. If not, compare pin 4 to the other five pins on U4. If pin 4 seems to behave properly and the others don't, then the problem is probably U2. If the reverse is true, then the problem is U3 or U9.

(b) Press and hold one of the scrolling keys--METER is a good choice. You should see continuous activity all along the main data path: continuous streams of pulses. Check the outputs of U4 (pin 9), U7A, U3B, U10D, and U12.

(c) You should also see continuous pulses on the three select lines coming out of U1 at pins 13, 14, and 15.

(d) Check for the presence of the 625 KHz FP CLOCK signal at pin 2 of U4, pin 5 of U3, and pin 12 of U10.

(e) Check that the clock line at pins 3 and 11 of U9 goes high and stays high as long as a key is held down.

(f) Check for a series of negative-going pulses on the FRONT PANEL ATTENTION line at the collector of Q1. Each pulse tells the microprocessor to read the key code from U4. One pulse is generated each time a key is

pressed; but when the key is held down, the pulses are continuous. The microprocessor responds by driving the KEYPAD-READ line low via U1 every time the key code is read, which results in a series of negative-going pulses corresponding to those on the FRONT PANEL ATTENTION LINE.

6-16. REPAIR OF THE DISPLAY ASSEMBLY, A1A11A2.

a Place the Display Assy A1A11A2 up side down on the Guide Assy and insure that the two ends capacitors of the Display Assy are inserted into the cavities of the Guide Assy.

b Unsolder the Back Light leads as required.

c Slide the Bracket Retainer (P/N 10085-2112) out of the Display Assy.

d Keep the Rubber Connector Trips (P/N 10085-5136) for possible reuse.

e Replace the LCD, Back Light, and Connectors Trips as required. Insure to clean the contact surface between the Connectors Trips and the Crystal display with Isopropyl Alcohol and soft cloth.

f Slide the Bracket retainer to it original position with the support of the Frame Assy. (Part of the Guide Assy)

g Solder four Back Light leads.

(1) Remarks.

The following drawings are needed to local manufacture the Guide Assy.

(a) Guide, Roller	Dwg#	20552
(b) Frame,	Dwg#	20554
(c) Block	Dwg #	20556
(d) Frame, Assy	Dwg #	20558
(e) Base, Assy	Dwg#	20553
(f) Spacer	Dwg#	20555
(g) Bolt/Bearing	Dwg#	20557
(h) Guide, Assy	Dwg#	20559

6-17. TRANSCEIVER CONTROL PWB ASSY, A1A12.

NOTE

The Transceiver Control PWB Assy contains the Intel 8088 microprocessor, which controls all the functions of the 100 Watt Transceiver, including the automatic BIT test. A failure in the microprocessor, EPROMs, RAMs, decoders, etc. will probably disable the BIT circuitry and most of the other transceiver functions as well. If the BIT circuitry is working, the only fault code associated with the Transceiver Control PWB Assy is 1A1A12-1, which indicates that there is a problem either with the power supply voltages (+15 Vdc and -15 Vdc) coming into the board or with the A/D Converter chip U7 that senses them. (The A/D Converter is used primarily with the metering and manual RF gain control circuitry. If it fails, it should not affect the essential functions of the transceiver, which are transmitting and receiving.) Unless you are thoroughly familiar with the circuitry of this board and with the operation of microprocessors, it will be very difficult for you to isolate a faulty chip or discrete component using standard test equipment and troubleshooting techniques. The following procedures, therefore, are intended to check only the most obvious and fundamental aspects of the board's operation. If these do not enable you to identify the problem, then you will need more advanced test equipment and test procedures, which are beyond the scope of this manual.

a. Checkout and Troubleshooting Procedures.

(1) Remove the good Transceiver Control PWB Assy from the test-bed 100 Watt Transceiver, and replace it with the fault Transceiver control PWB Assy.

(2) Power up the transceiver.

(3) Check the RESET signal at pin 21 of microprocessor U1. This pin should normally be low, but should go high when you push the reset button (S1).

(a) If the RESET signal is incorrect, check the reset circuitry: U41F, U10A, U10B, and U10C. Keep in mind that, in addition to the manual reset button, a RESET signal can be generated three other ways: (1) by a low voltage at TP1, which monitors the output of the +13.6 Vdc voltage divider circuit (if this voltage drops below +10 Vdc, a RESET will occur); (2) upon power-up, before the + input of U10C charges to a sufficient positive voltage to cause a high on pin 14, removing the RESET; and (3) by a low at pin 7 of U10B, which originates at pin 7 of the "Gone West Timer", U15. (The microprocessor must send a reset pulse to pin 1 of U15 every 13 ms, or U15 will generate a low at pin 7 after 65 ms, resetting the microprocessor. Check for negative-going reset pulses spaced 13 ms apart at pin 1 of U15.)

(b) If the RESET signal is okay, proceed to step 4.

(4) Check the CLOCK input to the microprocessor by connecting an oscilloscope to pin 19. Check for a 5 MHz square wave.

(a) If the CLOCK signal is missing or incorrect, check pin 9 Divide-by-Counter U12. If the signal is bad there, check the output of the 15 MHz Oscillator at pin 1 of U12.

(b) If the CLOCK signal is good, proceed to step 5.

(5) Check for the presence of the following voltages on the Transceiver Control PWB Assy:

Voltage:	Measure at:
+5 Vdc	+ side of C27
+15 Vdc	U39A, pin 8
-15 Vdc	U39A, pin 4
+13.6 Vdc	bottom of R3 (end away from potentiometer R2)

(6) Check the RAM disable line at pin 18 of U19 and U20. This line should normally be low, but should go high when you push the reset button. If this is not the case, check Bilateral Switch U14A. Pins 1 and 2 of this switch should be closed (at ground potential) when the microprocessor is not reset.

(7) Check for +5 Vdc at pin 24 of U19 and U20 with the transceiver turned on. With the transceiver turned off, the voltage at pin 24 of U19 and U20 should slowly diminish to +3.6 Vdc as the battery voltage is switched in.

(8) If all the above checks are good, replace microprocessor U1. (This chip is socketed for easy replacement.)

(9) If the problem persists, replace the EPROMs, U16-U18, then the RAMs, U19 and U20. (These chips are also socketed.)

(10) If the problem still persists, you can try checking the select lines to the EPROMs and RAMs from decoders U3 and U4A. One, and only one, of these lines should be low at any given time. If none of these lines goes low or if one or more lines are always low or if two or more go low at the same time, then there is a fault in the decoder.

(11) You can also check the select lines to the I/O devices at pins 7 and 9-15 of decoder U5. These lines should behave exactly like the select lines in step 10.

(12) As a final check, you can look at the clock signals on all the chips. Refer to the schematics for clock frequencies and pin locations.

6-18. LPA/COUPLER INTERFACE PWB ASSY, A1A13.

a. Preliminary Procedure.

(1) Remove the good LPA/Coupler Interface PWB Assy from the test-bed 100 Watt Transceiver, and replace it with the faulty LPA/Coupler Interface PWB Assy.

(2) Make sure that the transceiver is connected to a 100/500 Watt Antenna Coupler and a 500 Watt Linear Power Amplifier or to a 1000 Watt Antenna Coupler and a 1 KW Linear Power Amplifier. Make sure that the antenna coupler is connected to a dummy load capable of handling the output power of the power amplifier.

(3) Power up the system.

(4) Check for the presence of the two power supply voltages on the board:

Voltage:	Measure at:
+5 Vdc	+ side of C43
+13.6 Vdc	junction of R13, R18, and R21

(5) If the voltages check good, run the receive-transmit BIT test.

b. Interpreting the BIT Codes. Use the fault codes listed below as a guide in troubleshooting the LPA/Coupler Interface PWB Assy. In the event that the BIT test runs without generating a fault code, refer to the "Additional Symptoms" section following the fault code section.

BIT Test Description for
LPA/Coupler Interface PWB Assy

The test checks for the presence of the board by sending data to the board and receiving the MCB loopback bit in reply.

1A1A1-1

This code indicates that there is a problem in the RF MUTE signal line.

(1) With the system unkeyed, check for a high at pin 4 of U5B. Change the frequency on the transceiver by 1 MHz, then key the system. The voltage at pin 4 of U5B should go low, then high again.

(2) If this is not the case, check L16, C25 (for a short), U17A, U5B, L1, C12 (for a short), U17C, R20, and U2D.

(3) If pin 4 of U5B is good, check U17C and U2D.

1A1A13-0

This code indicates that the LPA/Coupler Interface PWB Assy did not respond to data from the Transceiver Control PWB Assy (did not send the MCB loopback bit).

Check the following components: U1, U5E, U8, U6, U9F. This is the signal path for the MCB loopback bit.

ADDITIONAL SYMPTOMS

(1) The LPA (Linear Power Amplifier) does not power up when commanded to by the 100 Watt Transceiver.

Check the LPA ON/OFF signal line as follows:

(a) The collector of Q6 should be 0 Vdc when the LPA is off and +13 Vdc when the LPA is commanded to turn on by the 100 Watt Transceiver.

(b) If this is not the case, check the signal at U8 pin 4 and U5C pin 5 (should be high when the LPA is commanded on and low when the LPA is commanded off). Check also the Q6 base circuitry (R4, R13, R18, and CR28).

(c) If this circuitry is okay, check for an open or a short on the line between Q6 and pin 27 of J3 (check for an open L7 or a shorted C4).

(2) The LPA powers up when commanded to by the transceiver, but no LPA status is displayed on the transceiver's front panel. The LPA cannot be turned off or controlled from the transceiver.

This indicates a fault in the UART circuitry. Check it as follows:

(a) Connect an oscilloscope to pin 4 of U4. You should see a data waveform (data pulses) when the LPA is commanded to turn on.

(b) If not, check for a low on pin 1 of U4, which indicates that transistor Q7 is turned on or shorted. If Q7 is on, then U4 is probably bad. If Q7 is off, the problem is probably in the collector circuit of Q7, in Q7 itself, or in the components between the base of Q7 and U13, including U13 itself.

(c) If pin 4 of U4 is good, check pin 20 of U13, which should be high with the LPA turned on and have low-going pulses when the LPA is given a command.

NOTE

In order to generate a data waveform, you must turn the LPA off and on or command it to switch from STANDBY to OPERATE.

If no data waveform was seen at pin 20 of U13, the problem is probably U2E or U14A.

(d) If pin 20 of U13 is good, check for the clock signal at pins 17 or 40 of U13. You should see a 78.6 KHz square wave.

(e) If the clock signal is present, the problem has to be U13, U10, U11, U3A, or U5D.

(f) If the clock signal is not present, the problem is in the UART clock oscillator/divider circuitry (U15,U16A,

U16B, U16F, and their associated components).

(3) The LPA powers up when commanded to by the 100 Watt Transceiver, the LPA status is displayed on the transceiver's front panel, but the LPA cannot be controlled (can't be commanded to go from STANDBY to OPERATE) from the transceiver.

(a) The problem is most likely in one of the following: U7B, U12, U2A, or U2C.

(b) To trace the data flow through these components, toggle the LPA between STANDBY and OPERATE.

(4) The coupler does not tune. This is indicated by one or more of the following symptoms:

- o The BYPASS message appears on the transceiver's display.
- o You cannot hear the coupler's tuning elements moving.
- o The meter on the transceiver and/or the LPA indicates a high VSWR.

(a) Check for the TUNE PULSE signal at the collector of Q5. This signal should be a momentary low when the transceiver is keyed, but high otherwise. If this signal is not correct, check U8, U9B, Q5, and their associated components.

(b) If the TUNE PULSE signal is good, check the KEY DISABLE line. This includes L16, U17A, U5B, U17C, U2D, and their associated components. This signal should go low when the mike is keyed and then go high again after the coupler reaches its home position and sends the TUNE POWER REQUEST signal.

(c) If the KEY DISABLE signal is good, check the TUNE POWER REQUEST signal line (pin 4 of J3 to L14 to pin 4 of U6). This signal is low and is issued by the coupler when it reaches its home position. The TUNE POWER REQUEST signal causes the KEY DISABLE signal to go high. The TUNE POWER REQUEST line goes high when the coupler becomes tuned.

(d) If all the above signals are good but the coupler does not tune, U6 or U9F is probably bad.

(5) Neither the coupler nor the LPA tunes when the system is keyed.

In this situation, the COND KEY line is the prime suspect. Check the circuitry between pin 4 of J2 and the collector of Q1. When the system is keyed, there should be a low at the cathode of CR4 and a high at the collector of Q1. When the system is not keyed, these points should be in the opposite logic states.

(6) When the system is keyed, the coupler tunes but the LPA doesn't.

Check the LPA KEY line: U5F and L3. This line should be low when the system is keyed and high when it isn't.

(7) When the system is keyed, the LPA tunes but the coupler doesn't.

Check the CPLR KEY line: U3E, R22, Q3, and L15. When the system is keyed, check for highs on pins 12 and 11 of U3E and lows on the base and collector of Q3. These signal levels should be reversed when the system is unkeyed.

6-19 MULTIVOLTAGE SUPPLY ASSY, A1A14.

a. Preliminary Procedure.

(1) Disconnect, but do not remove, the good Multivoltage Supply Assy in the test-bed 100 Watt Transceiver.

(2) In its place, connect the faulty Multivoltage Supply Assy.

(3) Power up the transceiver.

(4) Check the output voltages of the Multivoltage Supply Assy at the test points on the Interconnect PWB Assy:

TP1 (brown)	ground
TP2 (red)	-15 Vdc
TP3 (orange)	+15 Vdc
TP4 (yellow)	+13.6 Vdc
TP5 (green)	+5 Vdc

(5) The following are the most common cases of Multivoltage Supply Assy problems:

Case 1	All voltages are bad
Case 2	Only +5 V is bad
Case 3	Only +15 V is bad
Case 4	+5 V, +15 V are bad; -15 V is high
Case 5	Only -15 V is bad
Case 6	Voltages are too high
Case 7	Voltages are too low

(6) The troubleshooting procedures for the Multivoltage Supply Assy are based on an analysis of each of these cases. Refer to section b below.

b. Troubleshooting Procedures.

CASE 1
All voltages are bad.

(1) Check to see if fuse F1 (10 A slow blow) on the back of the transceiver is blown. If so, Q8 or Q9 on the Multivoltage Supply Assy could be shorted out. Proceed as follows:

(a) Unplug the Multivoltage Supply Assy from the transceiver.

(b) Check the resistance of pin 4 of Multivoltage Supply Assy plug P1 to ground.

(c) If the resistance measurement indicates a short, remove the cover of the Multivoltage Supply Assy.

(d) Remove the nuts holding the collector leads of power transistors Q8 and Q9.

(e) Check the transistors with an ohmmeter to see if they are shorted.

(2) If fuse F1 is not blown, turn off the transceiver and remove the cover from the Multivoltage Supply Assy. Then remove the circuit board and the EMI filter from the chassis.

(3) Power up the transceiver again, and check the collector of Q1. You should see approximately +13.0 Vdc from the 13.6 V Power Supply.

(4) If the voltage at the collector of Q1 is good, check pin 15 of U1 for approximately +14.3 Vdc.

(5) Check pins 12 and 13 of U1 for a 25 KHz square wave with an amplitude of 1.5 to 2 V pk-pk. The signals at pins 12 and 13 should be 180 out of phase. If this signal is good, skip to step 10.

NOTE

If the signal at pins 12 and 13 consists of narrow positive pulses, you have a possible current limit condition, which is indicated by +1.2 Vdc at the junction of R40, R44, and R39. If not, proceed to step 6. If there is a current limit condition, disconnect the wires to E2 and E3 and see if the voltage at these points returns to normal. If so, the problem is either in the EMI filter (check it with an ohmmeter) or in the current limit circuit (Q7 and its associated components). If disconnecting the E2 and E3 wires does not return the voltage to normal, check the resistance to ground from each point. If a short is indicated, trace it out. If not, the problem could be T3, Q8, Q9, or one of their associated components.

(6) If the signal at pins a low (less than +0.5 Vdc) at pin 10. If pin 10 is high, check pin 7 of AR1. If pin 7 of AR1 is high, either the incoming voltage is high (greater than +33 Vdc) or there is a problem with the AR1 circuitry.

(7) If the voltage at pin 10 of U1 is good (low), check for approximately +2.6 Vdc at pin 9. If pin 9 is low, check pin 1 of AR1. If pin 1 of AR1 is high, either the incoming voltage is low (less than +9 Vdc) or there is a problem with the AR1 circuitry. If pin 1 of AR1 is low,

there could be a problem with Q12, Q6, or one of their associated components.

(8) Check the voltage on pins 1 and 2 of U1. If pin 2 (which should be +2.5 Vdc) is higher than or equal to pin 1, then the voltage at pn 9 should be okay, unless there is a problem with U1 or the pin 9 line is shorted.

(9) If pin 2 does not read +2.5 Vdc, check for +5 Vdc at pin 16. If pin 16 does not read +5 Vdc, either U1 is bad or there is a bad component shorting the pin 16 line.

(10) Check the collectors of Q3 and Q4 for a 25 KHz square wave (not as clean as at pins 12 and 13 of U1) at an amplitude of at least 13 V pk-pk. If the signal is bad here, check for a fault in Q3, Q4, or one of their associated components.

(11) Check the collectors of Q8 and Q9 for the composite wave shown below (figure 6-20): The pk-pk amplitude should be twice the input voltage to the Multivoltage Supply Assy (or approximately 26 V). If this signal is good, skip to step 15.

(12) If the above signal is not present, check to see whether the line voltage (+13.0 Vdc from the 13.6 V Power Supply) is on the collectors of Q8 and Q9. If it isn't, skip to step 14. If it is, check the bases for a signal similar to the one in figure 6-21.

(13) If the above signal is present, Q8 or Q9 is probably bad. If it is not present, the problem is in T1 or its associated circuitry.

(14) If line voltage is not present at the collectors of Q8 and Q9, check for a problem with T3 or its associated wiring.

(15) Look at pin 1 of U2 for +15 Vdc. If this voltage is not present, there could be a problem in the secondary circuitry of T3 or in T3 itself.

(16) If the voltage at pin 1 of U2 is good, check E2, E3, and E6 for the proper output voltages. If good, the problem has to be in the wiring, the connector, or the EMI filter.

CASE 2
Only the +5 V is bad.

The problem is in the +5 V regulator circuit (U2 and its associated components). Check it as follows:

(1) Check for +15 Vdc at pin 1 of U2.

(2) Check for a 3.5 V pk-pk square wave at pin 7. If the signal is good, skip to step 4.

NOTE

If the signal at pin 7 of U2 consists of narrow pulses, you have a possible current limit condition, which is indicated by +0.5 Vdc at pin 6 of U2. If this is the case, disconnect the wire from E6. If the output voltage returns to normal, the EMI filter is probably bad. If the voltage does not return to normal, check for a short in Q10, Q11, T4, CR13, CR21, etc. If pin 6 of U2 does not indicate a current limit condition, check the zener voltage at pin 2 of U2 for +8.2 Vdc. Check to see that pin 3 is less than pin 2. If not, there is a problem either with U2 or its associated circuitry.

(3) Check for +4 to 4.5 Vdc at pin 4 and +3.7 Vdc (approximately) at pin 3. If these voltages are incorrect, troubleshoot the circuitry supplying them.

(4) Check the collector of Q13 for a pk-pk signal that is approximately 1.5 V. If it's not there, Q13 or its associated circuitry is bad.

(5) Check the collector of Q10 for a pk-pk signal equal to the supply voltage. If it's not there, check for a problem in Q10, Q11, or their associated components.

(6) Check E6 for +5 Vdc. If the voltage here is good, the EMI filter is probably bad. There could also be a problem in the wiring or the connector.

CASE 3
Only the +15 V is bad.

Check for a problem in the EMI filter or the wiring.

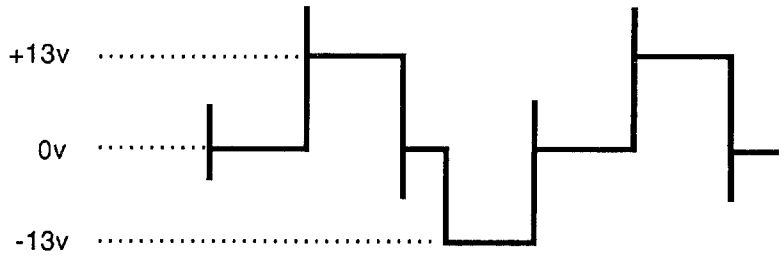


Figure 6-20. Composite Wave

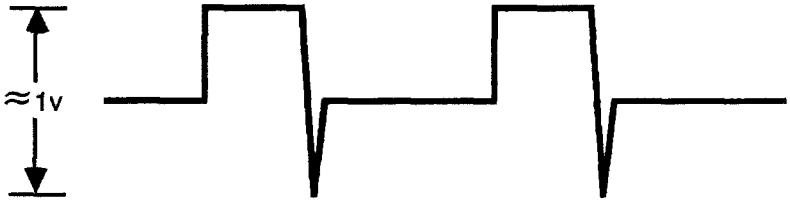


Figure 6-21. Base Signal for Q8, Q9